NETAJI SUBHAS UNIVERSITY, JAMSHEDPUR

Estd. Under Jharkhand State Private University Act, 2018
Approved by AICTE, PCI, BCI, NCTE, INC & JNRC

EVALUATION SCHEME & SYLLABUS

FOR
MASTER OF TECHNOLOGY
IN
Microelectronics and VLSI Technology
(M. TECH-MT)

On

Choice Based Credit System

(Effective from the Session: 2025-26)

Netaji Subhas University
Pokhari, Near Bhilai Pahadi, Jamshedpur, Jharkhand

VISION

To strive for excellence in education, research, and entrepreneurship, with the ultimate goal of becoming a global hub for innovation. Committed to advancing scientific and technological services, we aim to contribute meaningfully to society.

MISSION

- To provide high-quality education that nurtures innovation, entrepreneurship, and ethical values, shaping future professionals equipped for a globally competitive landscape.
- To collaborate with stakeholders by sharing institutional expertise in education and knowledge, fostering mutual growth in technical learning.
- To Cultivate an environment that encourages fresh ideas, groundbreaking research, and academic excellence, paving the way for future leaders, innovators, and entrepreneurs.
- To drive socio-economic progress by offering impactful scientific and technological solutions to society.

Program Outcomes (POs) and Program Specific Outcomes (PSOs)

A. Program Outcomes (Pos):

The following three POs for the PG programs:

PO 1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO 2: An ability to write and present a substantial technical report/document.

PO 3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

B. Program Specific Outcomes (PSOs):

Three program specific outcomes (PSOs) have been defined as follows -

PSO 1 (PO 4): Identify, formulate and solve engineering problems in the field of Microelectronics and VLSI

PSO 2 (PO 5): Apply knowledge, proper methodology and modern tools to analyze and solve the problems in the domain of Microelectronics and VLSI.

PSO 3 (PO 6): Acquire professional and intellectual integrity and ethics of research and recognize the need to engage in learning with a high level of enthusiasm and commitment to contribute to the community for sustainable development of society

Course Articulation Matrices: Connection between the courses and the POs and PSOs

The correlation levels are 1, 2 or 3, denoting:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High).

Curriculum for M. Tech. in Microelectronics & VLSI

SEMESTER I							
Sl. No	**Code**	**Subject**	**L**	**T**	**S**	**C**	**H**
1	MT/EC1011	Semiconductor Device & Modeling	3	0	0	3	3
2	MT/EC1012	Analog IC Design	3	1	0	4	4
3	MT/EC1013	Digital IC Design	3	0	0	3	3
4	MT/EC90XX	SPECIALIZATION ELECTIVE - I	3	1	0	4	4
5	MT/EC90XX	SPECIALIZATION ELECTIVE - II	3	1	0	4	4
6	MT/EC1061	Analog IC Design Lab	0	0	4	2	4
7	MT/EC1062	Digital IC Design Lab	0	0	4	2	4
		TOTAL	**15**	**3**	**8**	**22**	**26**

SEMESTER II							
Sl. No	**Code**	**Subject**	**L**	**T**	**S**	**C**	**H**
1	MT/EC2011	VLSI Technology	3	0	0	3	3
2	MT/EC2012	VLSI System Design	3	1	0	4	4
3	MT/EC90XX	SPECIALIZATION ELECTIVE - III	3	1	0	4	4
4	MT/EC90XX	SPECIALIZATION ELECTIVE - IV	3	1	0	4	4
5	MT/EC90XX	SPECIALIZATION ELECTIVE - V	3	1	0	4	4
6	MT/EC2061	VLSI System Design Lab	0	0	4	2	4
7	MT/EC2062	Term Project/ Lab-Based Project	0	0	6	3	6
		TOTAL	**15**	**4**	**10**	**24**	**29**

SEMESTER III							
Sl. No	**Code**	**Subject**	**L**	**T**	**S**	**C**	**H**
1	XX90XX	AUDIT LECTURES / WORKSHOPS	0	0	0	0	2
2	MT/EC3061	Project - I	0	0	24	12	24
3	MT/EC3062	SEMINAR - NON-PROJECT / EVALUATION OF SUMMER TRAINING	0	0	4	2	4
		TOTAL	0	0	28	14	30

SEMESTER IV							
Sl. No	**Code**	**Subject**	**L**	**T**	**S**	**C**	**H**
1	MT/EC4061	Project - II	0	0	24	12	24
1	MT/EC4062	PROJECT SEMINAR	0	0	4	2	4
		TOTAL	0	0	28	14	28

1. List of Electives:

Sl. No.	SUBJECT CODE	SUBJECT	L-T-S	CREDIT
1.	EC9030	Error Control Coding	3-1-0	4
2.	EC9031	Digital Signal Processing & its applications	3-1-0	4
3.	EC9032	Detection & Estimation Theory	3-1-0	4
4.	EC9033	Statistical Signal Processing	3-1-0	4
5.	EC9034	Image Processing	3-1-0	4
6.	EC9035	Queuing Theory for Telecommunication	3-1-0	4
7.	EC9036	Microwave & Millimeter Wave Circuits	3-1-0	4
8.	EC9037	Optical Communication	3-1-0	4
9.	EC9038	Antenna Analysis & Synthesis	3-1-0	4
10.	EC9039	Satellite Communication	3-1-0	4
11.	EC9040	Artificial Intelligence & Soft Computing	3-1-0	4
12.	EC9041	RF IC DESIGN	3-1-0	4
13.	EC9042	SoC Design	3-1-0	4
14.	EC9043	*FPGA based design	3-0-2	4
15.	EC9044	MEMS & Microsystem Technology	3-1-0	4
16.	EC9045	Embedded Systems	3-1-0	4
17.	EC9046	Internet of Things (IoT)	3-1-0	4
18.	EC9047	Nanoelectronics	3-1-0	4
19.	EC9048	*ASIC Design using Verilog/VHDL	3-0-2	4
20.	EC9049	Mixed Signal IC Design	3-1-0	4
21.	EC9050	Low Power Circuits and Systems	3-1-0	4
22.	EC9051	Testing and Verification of VLSI Circuits	3-1-0	4
23.	EC9052	Computer Architecture	3-1-0	4
24.	EC9053	Physical System Analysis and Modeling	3-1-0	4
25.	EC9054	Cyber Physical Electronic System Design	3-1-0	4
26.	EC9055	Electronic Measurements and System Design	3-1-0	4
27.	EC9056	DSP Architectures in VLSI	3-1-0	4
28.	EC9057	Power Management IC Design	3-1-0	4
29.	EC9058	Smart Materials based Electronic Devices	3-1-0	4

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***The Lecture, Tutorial and Laboratory/Sessional distribution of FPGA Based Design (MT/EC9043) and ASIC Design using Verilog/ VHDL (MT/EC9048) are 3, 0 and 2,respectively.**

2. Detailed Syllabus:

<table>
<tr><td colspan="8">Department of Electronics & Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total contact hours : 42</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC1011</td><td>Semiconductor Device & Modeling</td><td>PEL</td><td>3</td><td>0</td><td>0</td><td>3</td><td>3</td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After successful completion of the course, the student will be able to:
• CO 1: To introduce the physics of semiconductor materials for understanding the device modeling of semiconductor devices.
• CO 2: To understand the transport of charge carriers for the operation of semiconductor devices.
• CO 3: To apply suitable approximations and techniques to derive the physical model of semiconductor devices such as P-N junctions.
• CO 4: To analyze electrostatic variables and current-voltage characteristics of MOS devices under a variety of conditions.
• CO 5: To evaluate qualitative understanding of the physics of emerging MOS devices and conversion of this understanding into modeling.
• CO 6: To develop the fundamental understanding of device modeling and numerical simulation</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Semiconductor Electronics [L – 6; T - 0]
Semiconductor Materials, Band Model of Solids Thermal-Equilibrium Statistics, Carriers in Semiconductors, Drift Velocity, Mobility and Scattering, Drift & Diffusion Current, Device: Hall-Effect.
Module II. Metal-Semiconductor Contacts And P-N Junctions [L – 8; T - 0]
Metal-Semiconductor junctions, Current-Voltage Characteristics, Surface Effects. The pn junction, Step Junction, Linearly Graded Junction, Heterojunctions, Reverse-Biased p-n junctions and break down mechanism. Generation and Recombination.
Module III. Field-Effect Transistors (MOSFETs) and Its 1st order I-V Model [L – 9; T - 0]
MOS Capacitor, Flat Band Voltage, Oxide and Interface Charge, High and Low Frequency C-V Characteristics, Basic MOSFET behavior, Threshold Voltage Model, 1st Order I-V Model.
Module IV. Short Channel Effects and 2nd Order I-V Model [L – 10; T - 0]
Moore’s law, Technology nodes and ITRS, Physical & Technological Challenges to scaling short-channel effects: velocity saturation, device degradation, channel length modulation, body bias effect, threshold adjustment, mobility degradation, subthreshold current, hot carrier effects, velocity overshoot, high field effects in scaled MOSFETs, substrate current and effects in scaled MOSFETS.
Module V. Nonconventional MOSFETs [L – 5; T - 0]
High-k/metal gate, high mobility MOSFETS, SOI, Multi-gate MOSFETs, FinFET, GAA MOSFETs.
Module VI. Introduction to BSIM Modeling [L – 4; T - 0]
History of BSIM models, BSIM family of Compact device models, BSIM6 model, EKV Model, Introduction to the TCAD Simulation Tool, Examples of TCAD Simulations.</td></tr>
</table>

	Total Contact Hours: (L=42, T=0)= 42
Text Books, and/or Reference Material	**Text Books:** 1. Yuan Taur and Tak H. Ning, *"Fundamentals of Modern VLSI Devices*" 2nd Edition, Cambridge University Press, 2013. 2. Theodore I. Kamins Richard S. Muller, *"Device Electronics for Integrated circuits*", 3rd Edition Wiley, 2007. 3. Dragica Vasileska, Stephen M. Goodnick, and Gerhard Klimeck, "*Computational Electronics: Semiclassical and Quantum Device Modeling and Simulation*", CRC Press, 2010. 4. A B. Bhattacharyya, "*Compact MOSFET Models for VLSI Design*", Wiley-IEEE, 2009. **Reference Books:** 1. S. M. Sze and Kwok K. Ng., "*Physics of Semiconductor Devices*", 3rd Edition, John Wiley & Sons, 2002. 2. Robert F. Pierret, "*Semiconductor Device Fundamentals*", Pearson Education, 2006. 3. Donald A. Neamen, "*Semiconductor Physics and Devices*", 3rd Edition, Mc-Graw Hill, 2003. 4. Jasprit Singh, "*Semiconductor Devices- Basic Principles*", John Wiley and Sons Inc., 2001.

MT/EC1011: Semiconductor Device & Modeling
[Mapping between course outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	To introduce the physics of semiconductor materials for understanding the device modeling of semiconductor devices.	1	1	3	2	1	1
CO2	To understand the transport of charge carriers for the operation of semiconductor devices.	2	1	3	2	1	1
CO3	To apply suitable approximations and techniques to derive the physical model of semiconductor devices such as P-N junctions.	2	2	3	2	3	1
CO4	To analyse electrostatic variables and current-voltage characteristics of MOS devices under a variety of conditions.	2	2	3	3	2	1
CO5	To evaluate qualitative understanding of the physics of emerging MOS devices and conversion of this understanding into modeling.	2	2	3	3	3	2
CO6	To develop the fundamental understanding of device modeling and numerical simulation	3	3	3	3	3	2
Average		2.00	1.83	3.00	2.50	2.17	1.33

<table>
<tr><td colspan="7">Department of Electronics & Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Elective (PEL)</td><td colspan="4">Total contact hours : 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC1012</td><td>Analog IC Design</td><td>Elective (PEL)</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">]</td><td colspan="4"></td><td></td></tr>
<tr><td colspan="3"></td><td colspan="4"></td><td></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After successful completion of the course, the student will be able to:
• CO 1: Define various parameters/terms associated with MOS transistors and Analog IC design.
• CO 2: Describe the operation of a MOS transistor /Amplifier/other fundamental blocks.
• CO 3: Solve any given circuit using appropriate Large/Small Signal model equations.
• CO 4: Evaluate various performance metrics such as gain/BW/Power dissipation/Input & output range.
• CO 5: Analyze feedback circuit and determine its poles, zeros, gain margin & phase margin.
• CO 6: Design a Single stage Amplifier/Differential Amplifier to meet the given specifications.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. MOS Device Physics [L – 4; T - 2]
General Considerations, Overview of CMOS technology, MOS I/V Characteristics, Short Channel Effects, Noise, Large Signal MOS Device models.

Module II. MOS Models [L – 2; T - 1]
MOS Device Capacitance, Small Signal Device Models. Different trans-conductance (front gate: g_m, output: g_ds, back-gate: g_mb). Unity gain frequency calculation.

Module III. Single Stage Amplifiers [L – 8; T - 2]
Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage, Calculation of Amplifier parameters.

Module IV. Current Mirror [L – 3; T - 2]
Simple, Cascode, Wilson and Large Swing current mirrors; Constant g_m, Band gap references.

Module V. Differential Amplifiers [L – 7; T - 2]
Single Ended and double ended. Differential Operation, Basic Differential Pair, Common- Mode Response, Differential Pair with MOS loads, current mirror load.

Module VI. Frequency Response of Amplifiers [L – 6; T - 1]
General Considerations, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage, Differential Pair.

Module VII. Operational Amplifiers [L – 7; T - 2]
General Considerations, One Stage Op Amps, Two Stage Op Amps, Common – Mode Feedback(CMFB), Power Supply Rejection Ratio (PSRR) Input Range limitations(ICMR), Slew Rate, Noise and Offset in Op Amps.

Module VIII. Feedback [L – 5; T - 2]
Feedback-Types, Nyquist plot, Stability- Frequency compensation techniques, Miller compensation, pole splitting, Gain Margin, Phase Margin.

Total Contact Hours: (L=42, T=14)= 56</td></tr>
</table>

Text Books, and/or Reference Material	**Text Books:** 1. Behzad Razavi, "*Design of Analog CMOS Integrated Circuits*", McGraw-Hill, 2nd Edition 2017. 2. Adel Sedra, Kenneth C. Smith, Tony Chan Carusone, Vincent Gaudet, "*Microelectronic Circuits*", Oxford, 8th Ed. 2020 3. Franco Maloberti, "*Understanding Microelectronics: A Top-Down Approach*", Wiley 2011. **Reference Books:** 1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, "*Analysis and Design of Analog Integrated Circuits*", John Wiley & Sons, Inc., 5th Edition 2015. 2. Roubik Gregorian, Gabor C. Temes, "*Analog MOS Integrated Circuits for Signal Processing*", Wiley 1986.

MT/EC1012: Analog IC Design

[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	Define various parameters/terms associated with MOS transistors and Analog IC design.	2	1	2	3	1	1
CO2	Describe the operation of a MOS transistor /Amplifier/other fundamental blocks.	2	3	1	3	2	2
CO3	Solve any given circuit using appropriate Large/Small Signal model equations.	3	2	1	2	2	1
CO4	Evaluate various performance metrics such as gain/BW/Power dissipation/Input & output range etc.	3	1	1	3	2	1
CO5	Analyze feedback circuit and determine its poles, zeros, gain margin & phase margin.	3	1	1	2	1	2
CO6	Design a Single stage Amplifier/Differential Amplifier to meet the given specifications.	2	1	3	3	1	1
Average		**2.50**	**1.50**	**1.50**	**2.67**	**1.50**	**1.33**

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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC1013</td><td>Digital IC Design</td><td>PEL</td><td>3</td><td>0</td><td>0</td><td>3</td><td>3</td></tr>
<tr><td colspan="3">]</td><td colspan="5"></td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After successful completion of the course, the student will be able to:
• CO 1: Acquire idea about the digital IC design techniques.
• CO 2: Understand the characteristics of CMOS inverter.
• CO 3: Identify the basic steps of ASIC Design Flow and fabrication process.
• CO 4: Analyze the static and dynamic characteristics of CMOS circuits.
• CO 5: Design and implementation of combinational and sequential circuits.
• CO 6: Evaluate the performance of CMOS circuits.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Overview of VLSI Design [L – 6; T - 0]
Historical perspective, overview of VLSI design methodologies, VLSI design flow, design hierarchy, concepts of regularity, modularity, and locality, VLSI design styles, design quality, packaging technology, CAD technology, Recent Trends in VLSI Design & its research issues in industry: System case studies. Design automation of VLSI Systems: basic concepts. Deep Sub-micron Technologies: Some Design Issues.

Module II. MOS Transistor Theory [L – 4; T - 0]
Introduction to The metal oxide semiconductor (MOS) structure, Long-channel I-V characteristics, C-V characteristics, non-linear I-V effects, DC transfer characteristics, sub-threshold swing in MOSFET, multi-Vt.

Module III. ASIC Design Flow [L – 6; T - 0]
ASIC and SoC, Overview of ASIC flow, concepts of HDL coding, functional verification, RTL-GATE level synthesis, synthesis optimization techniques, pre-layout timing verification, static timing analysis, floor-planning, placement and routing, extraction, post layout timing verification, extraction.

Module IV. CMOS Process Technology [L – 2; T - 0]
Fabrication process flow- basic steps, the CMOS n-Well process, layout design rules, stick diagram, full-custom mask layout design.

Module V. MOS Inverter- Static Characteristics [L – 4; T - 0]
Resistive-load inverter, inverter with n-type MOSFET load, CMOS inverter.

Module VI. MOS Inverters- Switching Characteristics & Interconnects effects [L-6;T-0]
Delay-time definitions, calculation of delay times, logical efforts, inverter design with delay constraints, estimation of interconnect parasitics, calculation of interconnect delay, Bus vs. Network-on-Chip (NoC), switching power dissipation of CMOS inverters.

Module VII. Combinational CMOS Logic Circuits [L – 7; T - 0]
MOS logic circuits with depletion nMOS loads, CMOS logic circuits, complex logic circuits, CMOS transmission gates (pass gates), ratioed, dynamic and pass transistor logic circuits, domino circuits.

Module VIII. Sequential CMOS logic circuits [L – 7; T - 0]</td></tr>
</table>

	Behavior of bi-stable elements, SR latch circuits, clocked latch and flip-flop circuits, CMOS D-latch and edge-triggered flip-flop. Timing path, Setup time and hold time static, example of setup and hold time static, setup and hold slack, clock skew and jitter, Clock, reset and power distributions. **Total Contact Hours: (L=42, T=0)= 42**
Text Books, and/or Reference Material	**Text Books:** 1. N. H. E. Weste and C. Harris, "*Principles of CMOS VLSI Design: A System Perspective"*, 3rd Edition, Pearson Education 2007. 2. Sung-Mo Kang, Yusuf Leblebici, Chulwoo Kim, "*CMOS Digital Integrated Circuits*", 4th edition, McGraw-Hill, 2018. **Reference Books:** 1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", 2nd Edition, Pearson Education, 2009.

MT/EC1013: Digital IC Design

[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	Acquire idea about the digital IC design techniques.	1	1	2	2	3	2
CO2	Understand the characteristics of CMOS inverter	1	1	2	2	3	1
CO3	Identify the basic steps of ASIC Design Flow and fabrication process.	1	1	2	3	3	3
CO4	Analyze the static and dynamic characteristics of CMOS circuits	2	1	2	3	3	1
CO5	Design and implementation of combinational and sequential circuits	1	1	2	3	3	2
CO6	Evaluate the performance of CMOS circuits	1	1	2	3	3	1
Average		**1.17**	**1**	**2**	**2.67**	**3**	**1.67**

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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC2011</td><td>VLSI Technology</td><td>PEL</td><td>3</td><td>0</td><td>0</td><td>3</td><td>3</td></tr>
<tr><td colspan="3" rowspan="2"></td><td colspan="5"></td></tr>
<tr><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course, the student will be able to
• CO 1: Outline the basics of semiconductor crystal properties and growth process of Silicon wafer
• CO 2: Identify the fundamentals of IC fabrication
• CO 3: Illustrate the different methods involved in VLSI fabrication process
• CO 4: Appreciate the advanced methods involved in IC fabrication
• CO 5: Build the knowledge of process integration-NMOS, CMOS</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction [L – 2; T - 0]
History of IC’s; Operation & Models for Devices of Interest: CMOS and MEMS, Front End of Line (FEOL), Back End of Line (BEOL)

Module II. Electronic Materials and Clean Room Environment [L – 3; T - 0]
Crystal Structures, Defects in Crystals, Si, Poly Si, Si Crystal Growth, Definition of clean room, Need of Clean Room, RCA cleaning of Si.

Module III. Oxidation [L – 5; T - 0]
Dry and Wet Oxidation, Kinetics of Oxidation, Oxidation Rate Constants, Dopant Redistribution, Oxide Charges, Device Isolation, LOCOS, STI, Oxidation System.

Module IV. Lithography [L – 5; T - 0]
Overview of Lithography, Radiation Sources, Masks, Photoresist, Components of Photoresist Optical Aligners, Resolution, Depth of Focus, Advanced Lithography: E-beam Lithography, X-ray Lithography, Ion Beam Lithography.

Module V. Diffusion and Ion Implantation [L – 7; T - 0]
Pre-Deposition and Drive-in Diffusion Modeling, Dose, 2-Step Diffusions, Successive Diffusion, Lateral Diffusion, Series Resistance, Junction Depth, Irvin’s Curves, Diffusion System. Problems in Thermal Diffusion, Advantages of Ion Implantation, Applications in ICs, Ion Implantation System, Mask, Energy Loss Mechanisms, Depth Profile, Range & Straggle, Lateral Straggle, Dose, Junction Depth, Ion Implantation Damage, Post Implantation Annealing, Ion Channeling, Multi Energy Implantation.

Module VI. Thin Film Deposition [L – 6; T - 0]
Physical Vapor Deposition: Thermal evaporation, Resistive Evaporation, Electron beam evaporation, Laser ablation, Sputtering. Chemical Vapor Deposition: Advantages and disadvantages of Chemical Vapor deposition (CVD) techniques over PVD techniques, reaction types, Boundaries and Flow, Different kinds of CVD techniques: APCVD, LPCVD, Metallorganic CVD (MOCVD), Plasma Enhanced CVD etc.

Module VII. Etching [L – 2; T - 0]
Anisotropy, Selectivity, Wet Etching, Plasma Etching, Reactive Ion Etching.

Module VIII. Metallization/Interconnects [L – 5; T - 0]</td></tr>
</table>

	Overview of Interconnects, Contacts, Metal gate/Poly Gate, Metallization, Problems in Aluminum Metal contacts, Al spike, Electromigration, MetalSilicides, Cu metal lines, Multi-Level Metallization, Planarization, Inter Metal Dielectric. **Module IX. Etching [L – 7; T - 0]** NMOS, CMOS process, SOI process, 3D IC Process, Packaging. **Total Contact Hours: (L=42, T=0)= 42**
Text Books, and/or Reference Material	**Text Books:** 1. S. M. Sze, "*VLSI Technology*", 2nd Edition, McGraw Hill, 2003. 2. S. K. Gandhi, "*Silicon Process Technology*", 2nd Edition, Wiley India, 2009. **Reference Books:** 1. J. Plummer, M. Deal and P. Griffin, "*Silicon VLSI Technology*", 1st Edition, Pearson Education, 2009. 2. S. M. Sze and May, "*Fundamentals of Semiconductor Fabrication*", 2nd Edition, Wiley, 2004.

MT/EC2011: VLSI Technology

[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	Outline the basics of semiconductor crystal properties and growth process of Si wafer.	1	1	3	2	1	1
CO2	Identify the fundamentals of IC fabrication.	1	1	3	3	2	1
CO3	Illustrate the different methods involved in VLSI fabrication process	2	2	3	2	3	1
CO4	Appreciate the advanced methods involved in IC fabrication.	2	2	3	3	3	1
CO5	Build the knowledge of process integration-NMOS, CMOS.	3	3	3	3	3	1
Average		1.8	1.8	3	2.6	2.4	1

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC2012</td><td>VLSI System Design</td><td>PCR</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course, the student will be able to
• CO 1: Understand the full custom and semicustom design flow.
• CO 2: Learn about static timing analysis and design constraints.
• CO 3: Understand the design for testability flows.
• CO 4: Identify and interpret the design towards realizing VLSI design.
• CO 5: Design and analyse the performance (speed, power) of VLSI circuits and design for different specifications.
• CO 6: Evaluate and design of memory cell.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Overview of VLSI System Design [L – 2; T - 0]
VLSI System design methodologies, VLSI design flow, Recent Trends in VLSI Design & its research issues in industry: System case studies. Design automation of VLSI Systems: basic concepts. Deep Sub-micron Technologies: Some Design Issues.

Module II. Full Custom Flow [L – 6; T - 1]
Block specification, schematic design entry, netlist generation and simulation, simulation for process and operating corners, layout with DRC/ LVS clean, parasitic extraction for R & C, back annotation & simulation, simulation redone with parasitic information, Concepts of PCELL.

Module III. Constraints and Static Timing Analysis [L – 8; T - 3]
Basic tenets of synchronous static timing: setup & hold timing, multipath & false paths, clock skew & latency, Asynchronous and synchronous clocks, crossing clock domains & clock gating; Design a constraints for a design in SDC format: design objects, timing constraints, environmental constraints, case analysis; timing report, synchronous static timing.

Module IV. Semiconductor Memories [L – 8; T - 2]
Memory hierarchy and types; SRAM Cell optimization and design metrics, memory read and write path; DRAM array design and related constraints, DRAM interface- address decoding, pipelining, data interface, charge pumps; non-volatile memory cell-basic principle and operation, reliability considerations of NVM; Case study- high speed memory, low voltage memory.

Module V. Design for Testability [L – 8; T - 2]
Introduction to DFT, DFT directory structure, DFT rule checker, debugging and fixing DFT violations, scan Mapping, Scan mapping, scan chain connection, using pre-compiled cores, adding testability logic, ATPG, DFT flows.

Module VI. Flow for Designing Full SoC [L – 5; T - 3]
Block specification, schematic design entry, netlist generation and simulation, simulation for process and operating corners, layout with DRC/ LVS clean, parasitic extraction for R & C, back annotation & simulation, simulation redone with parasitic information, concepts of PCELL.

Module VII. Physical Design [L – 5; T - 3]
Floorplanning and placement, clock tree insertion & DFT insertion, routing, post PnR function</td></tr>
</table>

	& timing checks, interconnection architectures. **Total Contact Hours: (L=42, T=14)= 56**
Text Books, and/or Reference Material	**Text Books:** 1. N. H. E. Weste and C. Harris, "*Principles of CMOS VLSI Design: A System Perspective"*, 3rd Edition, Pearson Education 2007. 2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Second Edition, Pearson Education, 2016. **Reference Books:** 1. Michael L. Bushnell, Vishwani D. Agrawal, "*Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*", Kluwer Academic Publishers 2002. 2. Sung-Mo Kang, Yusuf Leblebici, "*CMOS Digital Integrated Circuits*", 3rd edition, Tata McGraw-Hill, 2003.

MT/EC2012: VLSI System Design

[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	Understand the full custom and semicustom design flow.	1	1	2	2	3	2
CO2	Learn about static timing analysis and design constraints.	1	1	2	2	3	1
CO3	Understand the design for testability flows.	1	1	2	3	3	3
CO4	Identify and interpret the design towards realizing VLSI design.	2	1	2	3	3	1
CO5	Design and analyse the performance (speed, power) of VLSI circuits and design for different specifications.	1	2	2	3	3	3
CO6	Evaluate and design of memory cell.	2	1	2	3	3	3
Average		**1.33**	**1.17**	**2**	**2.67**	**3**	**2.67**

A. Core Laboratories

Department of Electronics and Communication Engineering							
Course Code	Title of the course	Program Core (PCR) / Electives (PEL)	Total Number of contact hours				Credit
			Lecture (L)	Tutorial (T)	Practical (P)	Total Hours	
MT/EC1061	**Analog IC Design Lab**	**Core (Lab)**	0	0	4	4	2
]							

Course Outcomes	After going through the course, student will be able to • **CO1**: Operate CAD tools (Cadence/Mentor) to simulate Analog blocks in Modern CMOS process. • **CO2**: Determine the characteristics of active/ & passive devices for modeling and analysis. • **CO3**: Design an inverter (and other basic gates) based on the given specifications. • **CO4**: Optimize a differential amplifier to meet the target specification • **CO5**: Appreciate various performance metrics like CMRR, ICMR, PSRR, SR, Power Dissipation, Delay, and Noise Margin with respect to design variables. • **CO6**: Examine the effect of process variation using Monte Carlo simulation
Topics Covered/ Syllabus	**List of experiments:** 1. Determination of NMOS and PMOS characteristics 2. Determination of NMOS and PMOS device parameter (V_{T0}, k', λ, γ, SS) 3. Simulation of NMOS and PMOS Resistive Load Inverter. 4. Simulation of CMOS Inverter and measure its delay, Noise margin, power 5. Design of a voltage reference and simple, Cascode current mirror 6. Design & simulation of Common Source Amplifier 7. Simulation of Ring Oscillator. 8. Monte Carlo Simulation and process variation
Text/ Reference Materials	1. Behzad Razavi , "*Design of Analog CMOS Integrated Circuits*", McGraw-Hill 2. Cadence Tutorials : https://nano.wiki.ifi.uio.no/Cadence-Tutorial-English-cadence_6.1.6

MT/EC1061: Analog IC Design Lab [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	Operate CAD tools (Cadence/Mentor) to simulate Analog blocks in Modern CMOS process.	3	1	2	2	2	1
CO2	Determine the characteristics of active/ & passive devices for modeling and analysis.	1	1	3	3	3	1
CO3	Design an inverter (and other basic gates) based on the given specifications.	2	2	3	3	3	1
CO4	Optimize a Differential amplifier to meet the target specification	3	1	2	2	2	1
CO5	Appreciate various performance metrics like CMRR, ICMR, PSRR, SR, Power Dissipation, Delay, and Noise Margin with respect to design variables.	1	1	3	3	3	1
CO6	Examine the effect of process variation using Monte Carlo simulation	3	1	2	2	2	2
Average		**2**	**1.2**	**2.6**	**2.6**	**2.6**	**1**

Department of Electronics and Communication Engineering							
Course Code	Title of the course	Program Core (PCR) / Electives (PEL)	Total Number of contact hours				Credit
			Lecture (L)	Tutorial (T)	Practical (P)#	Total Hours	
MT/EC1062	**Digital IC Design Lab**	Core (Lab)	0	0	4	4	2

Course Outcomes	• **CO1:** Design a CMOS inverter to meet the given specifications. • **CO2:** Explain the CAD tool flow for Physical design of digital circuits. • **CO3:** Analyze the impact of device sizes in the implementation of CMOS circuits. • **CO4:** Design and implementation of combinational and sequential circuits • **CO5:** Evaluate the performance of CMOS digital circuits. • **CO6:** Draw the Layout of CMOS Circuits
Topics Covered	**List of experiments:** 1. Design and plot the static (VTC) characteristics of CMOS inverters. 2. Design and plot the dynamic characteristics of CMOS inverters. 3. Design and simulation of CMOS i) NAND, ii) NOR and ii) XOR gates. 4. Design and implementation of CMOS transmission gate and logic circuits using pass transistor logic (PTL). 5. Design a two-phase non-overlapping clock generator. 6. Design and implementation of dynamic and domino logic circuits. 7. Design and simulation of FFs (D, T, Master-slave) using pass transistors. 8. Design a 6T SRAM Cell and measure its characteristics. 9. Draw the Layout of CMOS i) Inverter ii) Transmission gate **Note: The simulations will be carried out using CMOS 180 nm and 65 nm process. For all the experiments, students need to measure and plot Static/dynamic power dissipation, Delay, Noise Margin, etc., for various loads. Results should also capture the impact of PVT variations.**
Text Books, and/or Reference Material	Suggested Text Books: 1. Eric Brunvand, "*Digital VLSI Chip Design with Cadence and Synopsys CAD Tools*", 2nd Edition, Pearson Education 2009. 2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Pearson Education, 2nd Edition, 2016.

MT/EC1062: Digital IC Design Lab
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	Design a CMOS inverter to meet the given specifications.	3	1	2	2	2	1
CO2	Explain the CAD tool flow for Physical design of digital circuits.	1	1	3	3	3	1
CO3	Analyze the impact of device sizes in the implementation of CMOS circuits.	2	2	3	3	3	1
CO4	Design and implementation of combinational and sequential circuits	2	2	3	3	3	1
CO5	Evaluate the performance of CMOS digital circuits.	2	2	3	3	3	1
CO6	Draw the Layout of CMOS Circuits	2	2	3	3	3	1
Average		**2**	**1.6**	**2.8**	**2.8**	**2.8**	**1**

Department of Electronics and Communication Engineering							
Course Code	Title of the course	Program Core (PCR) / Elective (PEL)	Total Number of contact hours				Credit
			Lecture (L)	Tutorial (T)	Practical (P)	Total Hours	
MT/EC2061	**VLSI System Design Lab**	Core-Lab	0	0	4	4	2

Course Outcomes	• **CO1**: Employ CAD tools to carry out Mixed Signal Design using bottom up approach • **CO2**: Illustrate gm/ID plots and its use in Analog Circuit Design • **CO3**: Design Opamps to meet any given specification. • **CO4**: Design and implementation of various components of a processor. • **CO5**: Evaluate the performance of VLSI Designs.
Topics Covered/ Syllabus	**List of experiments** : 1. Generation of gm/ID plots for various Channel lengths. 2. Design and optimize a two stage Opamp. 3. Design of Band-gap reference Circuit. 4. Design of 8 bit Flash ADC and measure its DNL, INL etc. 5. Design and implementation of ALU and ALU Controller. 6. Design and implementation of Sequence Controller. 7. Design and implementation of Multiplexer and Program Counter. 8. Design and implementation of Concentration, Combinational and shift-by-2 modules. 9. Design and implementation of RAM and Register files. 10. Design and implementation of State Register and Sign-Extend Modules.
Reference Materials	1. B. Razavi, "*Design of Analog CMOS Integrated Circuits"*, McGraw-Hill Education, 2002. 2. Allan Hastings, "*The Art of Analog Layout"*, Prentice Hall, Second Edition, 2005. 3. N. H. E. Weste and C. Harris, "*Principles of CMOS VLSI Design: A System Perspective*", 3rd Edition, Pearson Education 2007.

MT/EC2061: VLSI System Design Lab

[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	Employ CAD tools to carry out Mixed Signal Design using bottom up approach	1	1	2	3	3	1
CO2	Illustrate gm/ID plots and its use in Analog Circuit Design	2	2	2	3	3	1
CO3	Design Opamps to meet any given specification	2	2	2	3	3	1
CO4	Design and implementation of various components of a processor	3	2	3	3	3	1
CO5	Evaluate the performance of VLSI Designs.	3	3	3	3	3	2
Average		**2.2**	**2**	**2.4**	**3**	**3**	**1.2**

B. Electives

<table>
<tr><th colspan="8">Department of Electronics and Communication Engineering</th></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total contact hours: 57</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9030</td><td>Error Control Coding</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">• CO1: Acquire idea about different types of error control coding techniques.
• CO2: Understand generator matrix, encoding and decoding of different codes.
• CO3: Learn LDPC, BCH, RS and Turbo codes.
• CO4: Analyze and mitigate errors in channels.
• CO5: Differentiate between different coding strategies.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. (L – 8; T- 2)
Introduction to Linear Algebra: Group, Ring, Field, Vector Space.

Module II. (L – 9; T- 3)
Binary Linear Block Codes: Generator and Parity Check Matrices, Dual Codes, Decoding, General properties of linear block codes, Hamming Code.

Module III. (L – 6; T- 3)
Cyclic Codes: Algebraic description, Encoding and Decoding of Cyclic codes.

Module IV. (L – 4; T- 1)
BCH Codes: Properties, Encoding and Decoding.

Module V. (L – 3; T- 1)
Reed Solomon (RS) Codes: Definition, Decoding of RS codes.

Module VI. (L – 7; T- 2)
Convolution Codes: Definition, Encoding Trellis and State representation, Viterbi decoding, Error probability.

Module VII. (L – 3; T-1)
LDPC Codes: Definition, Construction, Regular and irregular LDPC, Belief Propagation, Tanner Graph, Decoding, Iterative Decoding

Module VIII. (L – 3; T- 1)
Turbo Codes: Definition, Construction methods, Decoding

Total Contact Hours: (L=43, T=14) = 57</td></tr>
<tr><td>Text Books, and/or Reference Material</td><td colspan="7">Text Books:
1. Shu Lin and Daniel. J. Costello Jr., Error Control Coding; Fundamentals and applications: 2nd Ed., Pearson India, New Delhi, 2010.
2. J. C. Moreira and P. G. Farrel, Essentials of Error Control Coding, 1st Ed., Wiley India, New Delhi, 2006</td></tr>
</table>

	Reference Books: 1. Todd.K. Moon, *Error Correction Coding: Mathematical Methods and Algorithm,* 1st Ed.,Wiley India, New Delhi, 2005.

MT/EC9038: Error Control Coding (Elective) **[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]**							
CO	**Statement**	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO 1**	**PSO 2**	
CO 1	Acquire idea about different types of error control coding techniques.	3	1	1	3	2	1
CO 2	Understand generator matrix, encoding and decoding of different codes.	2	2	2	3	1	2
CO 3	Learn LDPC, BCH, RS and Turbo codes.	2	2	1	3	1	2
CO 4	Analyze and mitigate errors in channels.	3	1	3	3	1	1
CO 5	Differentiate between different coding strategies.	1	1	2	3	2	2
Average		**2.2**	**1.4**	**1.8**	**3.0**	**1.4**	

<table>
<tr><th colspan="8">Department of Electronics and Communication Engineering</th></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total contact hours: 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9031</td><td>Digital Signal Processing & Application</td><td>Electives (PEL)</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">)</td><td colspan="6"></td></tr>
<tr><td colspan="2"></td><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">On successful completion of this course, students should have the skills and knowledge to:
• CO1: Analyse a given signal or system using tools such as Fourier transform and z-transform to know the property of a signal or system.
• CO2: Process signals to make them more useful; and how to design a signal processor for a given problem, construct simple IIR and FIR filter.
• CO3: Design and Analysis of various types of Analog Butterworth and Chebyshev Filters
• CO4: Design methods to convert analog filters into digital filters.
• CO5: Perform Frequency transformations in Analog and Digital domains. Realization of Digital FIR and IIR Filter Structure.
• CO6: Describe the operation of adaptive systems</td></tr>
<tr><td>Topics Covered/ Syllabus</td><td colspan="7">Module I. (L – 1)
Introduction: reasons behind digital processing of signals, brief historical development, organization of the course. [CO#1]

Module II. (L – 2)
Theory of discrete time linear system sequences, linear time invariant systems, causality, stability, difference equations, frequency response, discrete Fourier series, relation between continuous and discrete systems, Inverse Systems, Stability. [CO#1]

Module III. (L – 2; T - 1)
Z –transform: definition, properties of Z transform, system function, digital filter implementation from the system function, region of convergence in the Z plane, determining filter coefficients from the singularity locations, geometric evolution of Z transform in the Z plane, relationship between Fourier transform and Z transform, inverse Z transform. [CO#1]

Module IV. (L – 3; T - 1)
Transform technique: Fourier transform, its properties, inverse Fourier transform, discrete Fourier transform, properties of DFT, circular convolution, computations for evaluating the DFT, decimation in time and decimation in frequency, discrete Hilbert transform.

Module V. (L – 5; T - 2)
Digital filter structures: system describing equations, filter categories, All Pass Filters, Comb Filters, direct form I and II structures, cascade and parallel communication of second order systems, Polyphase representation of filters, linear phase FIR filter structures, Compensatory Transfer Functions, frequency sampling structure for the FIR filter. Test for Stability using All Pass Functions. [CO#1, 2]

Module VI. (L – 5; T - 2)
IIR filter design techniques: Analog Filter Design, Analog Butterworth lowpass filter design techniques, Analog Chebyshev LPF, Design methods to convert analog filters into digital filters, frequency transformation for converting lowpass filters into other types, all-pass filters for phase response compensation. [CO#2, 3]

Module VII. (L – 5; T - 2)
Digital Filter Structures: IIR Realizations, All Pass Realizations, FIR and IIR Lattice Synthesis, IIR Design by Bilinear Transformation, Digital to Digital Frequency Transformation. [CO#2, 3,4]

Module VIII. (L – 5; T - 1)
FIR filter design techniques: Windowing method for designing FIR filters, DFT method for approximating the desired unit sample response, combining DFT and window method for designing FIR filter, frequency sampling method for designing FIR filter [CO#2, 3]</td></tr>
</table>

	Module IX. (L – 5; T - 2) FFT- Derivation of the Radix-2 FFT: Describe the purpose of the Fast Fourier Transform (FFT) and explain its relationship with DFT, Outline the Fast Fourier Transform (FFT) in mathematical form using twiddle factors, Explain the properties of twiddle factors, Describe how the N-point sequence can be decomposed into N/2-point sequences and how the Discrete Fourier Transform (DFT) can be calculated, Explain the relationship between N-point DFT with N/2-point DFT of even and odd values of the signal, Outline the benefits of the radix method for FFT and its computational savings. **[CO#1,2]** **Module X. (L – 3; T - 1)** Adaptive Filters - Prediction and System Identification: Describe the characteristics of adaptive systems, Explain the functionality and operation of a closed-loop configuration involving adaptive filters, Explain the functionality and operation of a prediction configuration and system identification configuration involving adaptive filters, Outline applications for the system identification configuration with adaptive filters. **[CO#5]** **Module XI. (L – 3; T - 1)** Adaptive Filters - Equalization and Noise Cancellation: Explain the operation of the equalization configuration and the noise cancellation configuration involving adaptive filters, Outline applications for the equalization and noise cancellation configurations with adaptive filters, and Explain how noise cancellation works through adaptive filters. **[CO#4,5]** **Module XII. (L – 3; T - 1)** Adaptive Filters - Adaptive FIR filter and the LMS algorithm: Outline the operations of a basic adaptive Finite Impulse Filter (FIR) filter system in mathematical form, Explain the cost function of an adaptive Finite Impulse Filter (FIR) filter system, Outline the concept and purpose of the Steepest Descent and the Least Means Squares (LMS) algorithm, Discuss the pros and cons of using the LMS algorithm for adaptive FIR filtering. **[CO#2, 3, 4, 5]** **Total Contact Hours: (L=42, T=14)= 56**
Text Books, and/or Reference Materials	**Text Books:** 1. Alan V. Oppenheim, Ronald W. Schafer, and John R. Buck, "*Discrete-Time Signal Processing*", Second Edition, Pearson Education India. 2. John G. Proakis, Dimitris G. Manolakis, and D Sharma, "*Digital Signal Processing: Principles*", Algorithms and Applications, 3rd Edition, Pearson Education India. 3. Richard G. Lyons, "*Understanding Digital Signal Processing*", Prentice Hall, 1996. ISBN: 0201634678. 4. Sanjit K. Mitra, "*Digital Signal Processing: A Computer - Based Approach*", McGraw-Hill Higher Education 5. Tarun Kumar Rawat, "*Digital Signal Processing*", Oxford University Press, ISBN: 9780198081937 6. Donald S. Reay, "*Digital Signal Processing Using the ARM Cortex M4 Paperback*". **Reference Books/Materials:** 1. S. W. Smith, "*The Scientist and Engineer's and Guide to Digital Signal Processing*", California Technical Publishing, 1997. ISBN: 0-9660176-3. 2. Vinay K. Ingle, John G. Proakis, "*Digital Signal Processing using MATLAB*," Brooks/Cole-Thomson Learning 3. https://nptel.ac.in/courses/117/102/117102060/ 4. Digital Signal Processing using Arm Cortex-M based Microcontrollers: Theory and Practice https://www.arm.com/resources/education/textbooks/dsptextbook

MT/EC9031: Digital Signal Processing & Application (Elective) [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO 1	**PO 2**	**PO3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	Analyse a given signal or system using tools such as Fourier transform and z-transform to know the property of a signal or system.	3	2	1	3	2	1
CO 2	Process signals to make them more useful; and how to design a signal processor for a given problem, construct simple IIR and FIR filter.	1	2	1	1	1	1
CO 3	Design and Analysis of various types of Analog Butterworth and Chebyshev filters.	3	3	3	3	2	2
CO 4	Design methods to convert analog filters into digital filters.	3	3	3	2	2	2
CO 5	Perform Frequency transformations in Analog and Digital domains. Realization of Digital FIR and IIR Filter Structure.	3	3	2	3	3	3
Average		**2.6**	**2.6**	**2**	**2.4**	**2**	**1.8**

<table>
<tr><th colspan="8">Department of Electronics and Communication Engineering</th></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total contact hours: 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9032</td><td>Detection and Estimation Theory</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">)</td><td colspan="6"></td></tr>
<tr><td colspan="2"></td><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">• CO1: To familiarize students with Classical Statistical Inference Techniques and their applications to Communication and Signal processing
• CO2: To familiarize students with Signal Detection Theory
• CO3: To develop required mathematical skills for design and implementation of statistical signal processing algorithm</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Random Signal and Random Process Basics(L – 4; T - 1)
Important probability distribution functions: Gaussian, Chi-square, Rayleigh, Rician, Student’s t, F, Cauchy etc. Bivariate and Multivariate Distribution; Random Process, Correlation properties, Stationarity, Ergodicity, Gaussian Process, Power Spectral Density

Module II. Classical Decision Theory (L – 6; T - 2)
Introduction to signal detection problems; Bayes Criterion: Binary Hypothesis testing, M-ary hypothesis testing; Maximum Likelihood based Optimal detection, LRT(Likelihood ratio test) and performance. Neyman Pearson Criterion for optimal detection , Minimum probability of error detector, Minimax Criterion

Module III. Detection of Deterministic signal (L – 4; T - 2)
Matched Filter Detection, Optimal detection for white and Nonwhite noise, Multiple Hypothesis testing;

Module IV. Detection of Random Signal (L – 5; T - 1)
Estimator Correlator, Energy Detector;

Module V. Detection of Signal with unknown parameters (L – 5; T - 2)
Composite Hypothesis Testing : Bayesian Approach and GLRT, Sinusoidal detection;

Module VI. Minimum Variance Unbiased Estimation (L – 6; T - 2)
Introduction to signal Estimation, Minimum variance unbiased estimator (MVUE), Unbiased estimators, MVUE Criterion, Cramer Rao Lower bound (CRLB); General CRLB for signals in white noise.

Module VII. Random parameter Estimation: (L – 6; T - 2)
Bayesian Formulation, Minimum mean square error (MMSE) and MAP estimation,Linear MMSE estimation, Wiener and optimum MMSE Filtering;

Module VIII. Non-Random Parameter Estimation: (L – 6; T - 2)
Least squares estimation, Best linear unbiased estimation (BLUE), Geometric interpretations, Maximum likelihood Estimation, Efficiency and consistency of estimators and asymptotic properties

Total Contact Hours: (L=56, T=0)= 56</td></tr>
<tr><td>Text Books, and/or Reference</td><td colspan="7">Text Books:
1. Fundamentals of Statistical Signal Processing, (Vol 1 & Vol 2), S.M. Kay, Pearson
2. Detection, Estimation, and Modulation Theory, Part-1, VanTrees, Jhon Wiley</td></tr>
</table>

Material	Reference Books:
	1. Signal Detection and Estimation, Second Edition, Mourad Barkat Artech house. 2. An Introduction to Signal detection and Estimation: H. Vincent Poor, Springer-Verlag

MT/EC9032: Detection and Estimation Theory (Elective) [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	To familiarize students with Classical Statistical Inference Techniques and their applications to Communication and Signal processing	3	3	3	3	1	2
CO 2	To familiarize students with Signal Detection Theory	3	3	3	3	1	2
CO 3	To develop required mathematical skills for design and implementation of statistical signal processing algorithm	3	3	3	3	1	3
Average		3	3	3	3	1	2.33

<table>
<tr><th colspan="8">Department of Electronics and Communication Engineering</th></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9033</td><td>Statistical Signal Processing</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO1: Understanding statistical models in the analysis of signals using Stochastic processes
CO2: To familiarize students with application of hypothesis testing to signal and event detection problems.
CO3: Design and development of optimum filters using classical and adaptive algorithms.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module 1. Background and Preview (L – 4, T – 1)
The filtering problem, Linear Optimum Filters, Adaptive Filters, Linear Filter Structures, Approaches to develop linear adaptive filters, Adaptive Beamforming (4L)

Module 2. Stochastic Processes and Models(L – 6, T – 2)
Partial characterization of a discrete-time stochastic process, Mean Ergodic Theorem, Correlation Matrix, Stochastic models, Wold decomposition, Asymptotic stationarity of an autoregressive process, Yule-Walker eqns., complex Gaussian Process, Power Spectral Density and its properties, transmission of stationary process through a linear filter, Power spectrum estimation.

Module 3. Weiner Filters: (L – 3, T – 1)
The statement of Linear Optimum Filtering, Principle of Orthogonality, minimum mean-square error, Wiener-Hopf equations (3L)

Module 4. Linear Prediction: (L – 5, T – 2)
Forward Linear Prediction, Backward Linear Prediction (3L), Levinson-Durbin Algorithm, Properties of prediction-error filters, Autoregressive modelling of a stationary random process, Cholesky Factorization, Lattice Predictors, All-pole, All-pass Lattice Filter

Module 5. Method of Steepest Descent: (L – 3, T – 1)
Basic idea of steepest descent algorithm, Steepest descent applied to Wiener filter, stability, Examples

Module 6. Least-Mean-Square (LMS) Adaptive Filters: (L – 5, T – 2)
Structure and operation of LMS algorithm, LMS Adaptation algorithm, Statistical LMS theory, comparison between LMS algorithm and steepest descent algorithm, directionality of convergence of the LMS algorithm for non-white inputs, Robustness of the LMS Filter, bounds on step size, transfer function approach for deterministic inputs, Normalized LMS Adaptive filters

Module 7. Method of Least Squares: (L – 5, T – 2)
Statement of Least Squares Estimation problem. Data windowing, Minimum sum of error squares, Normal Equations and Linear Least Squares Filters, Time-Averaged correlation matrix, Properties of Least Squares estimates, Singular Value Decomposition (SVD), Pseudo-inverse, Interpretation of singular values and singular vectors, Minimum-Norm solution to the Linear Least Squares problem

Module 8. Recursive Least Squares (RLS) Adaptive Filters: (L – 5, T – 2)
Matrix Inversion Lemma, Exponentially weighted RLS algorithm, selection of the regularizing parameter, Update recursion for the Sum of Weighted Error Squares, Example of a single weight</td></tr>
</table>

	adaptive noise canceller, convergence analysis of the RLS algorithm, Robustness of RLS Filters **Module 9. Kalman Filters**: **(L – 5, T – 2)** Recursive MMSE for scalar random variables, Statement of the Kalman Filtering problem, The Innovations process, Estimation of the state using Innovations process, Filtering, Initial Conditions, Kalman Filter as the unifying basis for RLS Filters, Kalman Filter variants, the Extended Kalman Filter **Total Contact Hours: (L=41, T=15)= 56**
Text Books, and/or Reference Material	**Text Books:** 1. Fundamentals of Statistical Signal Processing: Estimation Theory - Steven M. Kay 2. Adaptive Filter Theory - Simon Haykin (Fourth Edition) **Reference Books:** 1. Statistical Digital Signal Processing and Modeling - Monson H. Hayes 2. Probability, Random Variables and Stochastic Processes - Athanasios Papoulis and S. Unnikrishna Pillai 3. An Introduction to Statistical Signal processing, Gray and Davisson, Cambridge University Press

MT/EC9033: Statistical Signal Processing
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Understanding statistical models in the analysis of signals using Stochastic processes	3	2	3	3	1	2
CO 2	To familiarize students with application of hypothesis testing to signal and event detection problems.	3	2	3	3	1	2
CO 3	Design and development of optimum filters using classical and adaptive algorithms.	3	2	3	3	1	3
Average		3	2	3	3	1	2.33

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total contact hours: 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9034</td><td>Image Processing</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">• CO1: Understand image enhancement and restoration techniques.
• CO2: Analyze digital images through multiresolution techniques.
• CO3: Understand the application of morphological processing and segmentation in digital images.
• CO4: Interpret digital image recognition techniques.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Digital Image Fundamentals[L – 4; T – 1]
Image acquisition, Sampling, Quantization, Resolution, Relationship between pixels, Geometric transforms, Convolution and Correlation.

Module II. Image Enhancement [L – 6; T – 2]
Gray level intensity transforms, Histogram processing, Image sharpening and smoothening operations (spatial and frequency based)

Image Restoration[L – 6; T – 2]
Model of image degradation, Noise models, Restoration in the presence of noise only spatial filtering, Periodic noise reduction by frequency domain filtering, Estimating the degradation function, Weiner filtering, Constrained least squares filtering, Image interpolation and resampling.

Module III. Multi-resolution Image Processing [L – 5; T – 2]
Short time Fourier transform, Wavelet function, Wavelet series, Discrete wavelet transform and multi-resolution analysis, Image decomposition and compression using discrete wavelet transform.

Module IV. Compression and Encoding of Image [L – 6; T – 2]
Redundancy, Entropy coding, Lossy compression, Lossless compression, Quality preserving adaptive compression.

Module V. Morphological Processing [L – 5; T – 1]
Dilation and erosion, Opening and closing, Hit or Miss transform, Algorithms for feature extraction.

Module VI. Image Segmentation: [L – 6; T – 2]
Detection of discontinuities, Edge linking and boundary detection, Thresholding, Region based segmentation, Segmentation by morphological watersheds, Use of motion in segmentation.

Module VII. Patterns in Images and their Applications [L – 4; T – 2]
Basics of features, Principal component analysis, Decision tree and feature hierarchy, Scale invariant feature transform, Histogram of oriented gradient.
Total Contact Hours: (L=42, T=14)= 56</td></tr>
<tr><td>Text Books, and / or Reference</td><td colspan="7">Text Books:
1. R C Gonzalez and R E Woods, Digital Image Processing, 4th Edition, Pearson, 2018.</td></tr>
</table>

Material	2. A Das, *Guide to Signals and Patterns in Image Processing- Foundations, Methods and Applications*, 1st Edition, Springer, 2015. 3. M Sonka, R Boyle, and V Hlavac, *Digital Image Processing and Computer Vision*, 1st Edition, Cengage Learning India, 2008. **Reference Books:** 1. K R Castleman, *Digital Image Processing*, 2nd Edition, Pearson India, 2011. 2. S Sridhar, *Digital Image Processing*, 2nd Edition, Oxford University Press, 2016.

MT/EC9034: Image Processing (Elective)
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	**Understand** image enhancement and restoration techniques	3	3	3	3	3	2
CO 2	**Analyze** digital images through multiresolution techniques	3	3	3	3	3	2
CO 3	**Understand** the application of morphological processing and segmentation in digital images	3	3	3	2	2	2
CO 4	**Interpret** digital image recognition techniques	3	3	3	3	2	2
Average		**3**	**3**	**3**	**2.75**	**2.5**	**2**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9035</td><td>Queuing Theory for Telecommunication</td><td>PEL (Program Elective)</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="5"></td></tr>
<tr><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="6">CO1: To understand the concept of queuing models and apply in Engineering
CO2: To understand significance of advanced queuing theory in Communication Networks
CO3: To develop expertise to analyse and design Communication Networks</td></tr>
<tr><td>Topics Covered</td><td colspan="6">Module I. Review of Probability Concepts [L – 5; T – 2]
Random variables, Binomial, Geometric, Poisson, Exponential, Gamma, Normal, Moments of random variables, Moment Generating Functions, Markov’s inequality, Chebyshev’s inequality, Laws of large number, Transformation of random variables.
Module II. Poisson Process [L – 6; T – 2]
Exponential distribution and memoryless property, Counting process, Inter arrival and waiting time distribution, Properties of Poisson process, Non homogeneous Poisson, Compound Poisson process, sum of independent Poisson, random splitting of Poisson process.

Module III. Markov Chains and Renewal Theory [L – 9; T – 3]
Discrete time Markov Chain, Chapman Kolmogorov Equation, Limiting probabilities, Time reversal Markov Chains, Continuous time Markov Chain, Birth Death process, Transition probability function, Computation of Transition Probability, Reward Renewal Process, Semi Markov process, Regenerative Process.

Module IV. Markovian Queues [L – 9; T – 3]
Queuing process, system performance, Notation for Queuing Systems, Little’s Formula, Analysis of M/M/1, M/M/1/K, M/M/S, M/M/S/S, Queues with unlimited service (M/M/∞ queues). Distribution of queuing delays in FIFO case, M/M/1 and M/M/S cases Erlang’s Formula M/M/S/S, M/M/S; Queues with parallel channels and Truncation (M/M/S/K)

Module V. Non-Markovian Queues [L – 9; T – 3]
Poisson input General service Time model, Poisson input Constant Service time model. Queuing system with Bulk service. Analysis of M/G/1, M/D/1, M/G/1 system with delay distribution. Generalization of M/G/1 Theory. M/G/1 with geometrically distributed message. M/G/1 with random size batch arrival.

Module VI. Network of Queues [L – 4; T – 1]
Traffic rate equation, Little Theorem for whole network, Burke Theorem, Jackson Theorem, Priority Queues

Total Contact Hours: (L=42, T=14)= 56</td></tr>
<tr><td>Text Books, and/or Reference Material</td><td colspan="6">Text Books:
1. Fundamentals of Queuing Theory: Gross and Harris, John Wiley & Sons
2. Queuing Theory and Telecommunications Networks and Applications: Giovanni Giambene, Springer
Reference Books:
1. Data Networks – D. Bertsekas and R. Gallager (Prentice Hall).
2. Introduction to Queuing Networks, Theory and Practice – Smith, J. MacGregor (Springer).
3. Teletraffic Theory and Applications: Haruo Akimaru and KonosukeKawashima,Springer
4. Introduction to Probability Models: Sheldon M. Ross, Academic Press</td></tr>
</table>

	5. Probability & Statistics with Reliability Queuing and Computer Science Applications: Kishore Trivedi, Wiley

MT/EC9035 Queuing Theory for Telecommunication [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	Statement	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	To understand the concept of queuing models and apply in Engineering	**3**	**3**	**3**	**3**	**1**	**2**
CO2	To understand significance of advanced queuing theory in Communication Networks	**3**	**2**	**3**	**3**	**1**	**1**
CO3	To develop expertise to analyse and design Communication Networks	**3**	**2**	**3**	**3**	**1**	**1**
Average		**3**	**2**	**3**	**3**	**1**	**1.33**

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<tr><th>Lecture (L)</th><th>Tutorial (T)</th><th>Practical (P)</th><th>Total Hours</th></tr>
<tr><td>MT/EC9036</td><td>Microwave and Millimeter wave Circuits</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">● CO1: Students will be able to learn the intricacies of design constraints at high frequency.
● CO2: The basic training for understanding circuit design at microwave frequencies for our Country's defense and space applications would be enriched.
● CO3: The students can design planar circuits and can provide reasoning for the obtained results.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction: [L – 2; T – 1]
Microwave and mm wave spectrum, Typical applications of microwave and mm wave, Safety considerations. Difference in High frequency and relatively low frequency behaviour of Lumped circuit components. Miniaturization and design of Lumped components at high RF. Realization of reactive elements as microwave and mm wave planar circuit components.[1][2]

Module II. Review of Transmission line theory. Concept of Scattering Matrix[L – 4; T – 2]
N-port networks-Properties of S matrix, Transmission matrix and their relationships

Module III. Microwave and mm wave Waveguide and Resonators [L – 6; T – 2]
Rectangular Waveguide- design consideration, TE and TM modes, TE_{10} mode analysis, cut-off frequency, propagation constant, intrinsic wave impedance, phase and group velocity, power transmission, attenuation, waveguide excitation, wall current; Introduction of circular waveguide; Rectangular waveguide resonator design consideration, resonant frequency, Q-factor, excitation.[1][3]

Module IV. Planar Transmission lines and Resonators [L – 6; T – 2]
Propagation characteristics, comparison for different characteristics of the above mentioned lines. strip line, micro-strip line, coplanar waveguide, Slot line-design consideration, Substrate integrated waveguide, non radiating dielectric guides, Design synthesis and analysis[1][2]

Module V. Passive Components and their S-matrix Representation [L – 8; T – 2]
Microwave and mm wave passive components and their S matrix representation: Attenuators, Phase shifter, Directional coupler, Bethe-hole coupler, magic tee, hybrid ring, circulators, Isolators; design of planar power dividers and couplers; design procedure of filter using insertion loss method-specification, low-pass prototype design, scaling and conversion, implementation. [2][3]
Module VI. Microwave and mm wave devices and Application to switches and mixers [L – 6; T – 2]
TED (Gunn diode) & Avalanche Transit Time (IMPATT) device, Schottky diode, PIN & applications; Microwave bipolar transistor, Microwave field effect transistor. [2]
Module VII. Microwave Amplifier Design [L – 6; T – 2]
Basic consideration in the design of microwave amplifier- transistor S-parameter, Stability, matching network, noise figure; matching network design using lumped elements and L-Section. Design of LNA.[1][4]
Module VIII. Microwave and mm wave measurement basics [L – 4; T – 1]
VSWR meter, tunable detector, slotted line and probe detector, spectrum analyzer, network analyzer,</td></tr>
</table>

	measurement of VSWR – low, medium and high, measurement of power: low, medium and high, frequency measurement.[1][4] **Total Contact Hours: (L=42, T=14)= 56**
Text Books, and/or Reference Material	**Text Books:** 1. David. M. Pozar, "*Microwave Engineering"*, 2/e, 1998 (John Wiley & Sons). 2. R Ludwig and P Bretchko, "*RF Circuit Design: Theory and Application"*, Pearson Education, New Delhi 3. Samuel Y Liao, "*Microwave Devices and Circuits"*, 3/e, PHI. 4. Sorin Voinigescu, "*High Frequency Integrated Circuits"*, Cambridge University Press, UK, 2013 5. G H Bryant, "*Principles of microwave Measurement"*, London : P. Peregrinus Ltd. on behalf of the Institution of Electrical Engineers, c1988 **Reference Books:** 1. P A Rizzi, "*Microwave Engineering: Passive Circuits"*, 2000, PHI 2. R E Collin, "*Foundations of Microwave Engineering"*, John Wiley and Sons India Pvt. Ltd.

MT/EC9036: Microwave Circuits & Techniques (Elective) [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	Statement	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO 1	Students will be able to learn the intricacies of design constraints at high frequency.	2	1	2	2	3	1
CO 2	The basic training for understanding circuit design at microwave frequencies for our Country's defense and space applications would be enriched.	2	3	1	1	3	1
CO 3	The students can design planar circuits and can provide reasoning for the obtained results.	3	2	1	1	3	1
Average		**2.3**	**2.0**	**1.3**	**1.3**	**3.0**	**1.0**

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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9037</td><td>Optical Communication</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="2"></td><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">● CO1: Students will be able to learn the intricacies of design constraints at optical frequency.
● CO2: The basic training for understanding circuits and system level implementation in lightwave technology.
● CO3: The students can design components and choose appropriate sources and receivers for an optical network.
● CO4: Understanding the usage of OTDR in monitoring an optical communication system.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction to optical communication: [L – 2; T – 0]

Overview of general communication, advantages of optical communication; Shannon noiseless coding theorem and Shannon noisy coding theorem.

Module II. Optical Fiber:[L – 8; T – 2]

Classification of Fibers, Fiber materials and fabrication methods, Ray optics representation and wave optics representation for step index and graded index fibers, Modes, Phase and group velocity, Power flow in step index fibers.

Module III. Propagation Characteristics in Optical Fibers: [L – 8; T – 2]

Signal attenuation in fiber, dispersion, classification and effect of dispersion in information transfer, review of fiber connectors, couplers, optical filter, isolator, circulator and attenuator.

Module IV. Design aspects of optical communication:[L – 8; T – 1]

optical fiber systems, modulation schemes, digital and analog fiber communication system, system design consideration, emitter and detector design, fiber choice, connectors, various amplifiers and its characteristics; OTDR

Module V. Optical transmitter: [L – 4; T – 1]

Basic concepts, characteristics of semiconductor injection LASER, LED, transmitter design

Module VI. Optical Receiver: [L – 6; T – 2]

Basic concepts, p-n and p-i-n photo detectors, Avalanche photo detectors, MSM photo detector, receiver design, receiver noise, receiver sensitivity, optical amplifier and its applications; Direct detection; Coherent communication: Basic concept, detection principles, practical considerations, modulation and demodulation schemes, heterodyne and homodyne detection, single and multicarrier systems, DPSK system.

Module VII. Wavelength division multiplexing (WDM):[L – 5; T – 1]

Multiplexing techniques, topologies and architectures, wavelength shifting, WDM demultiplexer,</td></tr>
</table>

	optical add/drop multiplexers. **Module VIII. Dense wavelength division multiplexing (DWDM): [L – 5; T – 1]** System considerations, multiplexers and demultiplexers; Fiber amplifier for DWDM, SONET/SDH transmission, modulation formats, NRZ and RZ signaling, DPSK system modeling. Potential applications and future prospects of optical fibers, multimode intensity sensors and single mode, Interferometric sensors. Recent trends in optical communication. **Total Contact Hours: (L=42, T=14)= 56**
Text Books, and/or Reference Material	**Text Books:** 1. J. M. Senior, "*Optical Fiber Communications*", PHI, 2nd Ed., 2005. 2. G. Keiser, "*Optical Fiber Communication*", McGraw Hill, 3rd Ed., 2008. 3. Ghatak & Thyagarajan, "*Introduction to fiber Optics*", Cambridge University press, 2000. 4. Henry Zanger and Cynthia Zanger, "*Fiber Optics Communication and Other Application"*, Macmillan Publishing Company, Singapore 1991. **Reference Books:** 1. J. H. Franz & V.K.Jain, "*Optical Communications*", Narosa Publishing House. 2. Ghatak & Thyagarajan, "*Contemporary Optics*", Series Title: Optical Physics and Engineering, Springer, 2000. 3. Amnon Yariv and Pochi Yeh, "*Photonics: Optical electronics for Modern Communication*", 6th Ed., New York, Oxford University Press, 2003.

MT/EC9037: Optical Communication
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	Students will be able to learn the intricacies of design constraints at optical frequency.	**1**	**1**	**2**	**2**	**3**	**1**
CO2	The basic training for understanding circuits and system level implementation in lightwave technology.	**3**	**2**	**3**	**2**	**1**	**2**
CO3	The students can design components and choose appropriate sources and receivers for an optical network.	**2**	**1**	**3**	**1**	**2**	**1**
CO4	Understanding the usage of OTDR in monitoring an optical communication system.	**2**	**2**	**3**	**2**	**2**	**2**
Average		**2**	**1.5**	**2.75**	**1.75**	**2**	**2**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9038</td><td>Antenna Analysis & Synthesis</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3" rowspan="2"></td><td colspan="5"></td></tr>
<tr><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After successful completion of the course, the student will be able to:
• CO 1: Ability to characterize resonance and radiation property of an antenna based on application
• CO 2: Learn various design parameters that affects an antenna and antenna array patterns.
• CO 3: Understand different types of antenna based on the radiation mechanism like wire antenna, aperture antennas, traveling wave antenna.
• CO 4: Understand different types of antenna based on the design mechanism like log periodic antenna, log spiral antenna and electrically long antenna as well as electrically small antenna.
• CO 5: Design suitable antenna feeding mechanism as well as matching mechanism.
• CO 6: Analyze and synthesize different types of antennas for different wireless communications.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Brief review on antenna fundamentals [L – 3; T - 1]
Antenna fundamentals; Vector potentials and solution of the vector potential wave equation; Antenna theorems and definitions.

Module II. Radiation theory and derivation of radiation parameters [L – 6; T - 2]
Dipole, loop antennas, Chu’s limit; Log-periodic antenna, Log spiral principle.

Module III. Antenna Array design and characterization [L – 6; T - 2]
Linear, planar and circular array - theorems and pattern synthesis.

Module IV. Integral Equations[L – 3; T - 1]
Moment method, self and mutual impedances

Module V. Scanning antennas [L – 6; T - 2]
Signal processing antennas, travelling wave and broadband antenna; Concept of smart antennas.

Module VI. Microstrip antennas [L – 6; T - 2]
Operating principle, modes, field patterns, impedance, feeding techniques and polarization; Arrays and feed networks.

Module VII. Aperture antennas [L – 6; T - 2]
Huygen’s principle, Babinet’s principle; Fourier transform theory and its applications; The Geometrical theory of diffraction and uniform theory of diffraction techniques and their applications.

Module VIII.Antenna measurements[L – 6; T - 2]
Antenna ranges, Impedance Measurements, Radiation Patterns, Gain Measurements, Directivity Measurements, Radiation Efficiency, Current Measurements, Polarization Measurements.

Total Contact Hours: (L=42, T=14)= 56</td></tr>
</table>

Text Books, and/or Reference Material	**Text Books:** 1. C. A. Balanis, *Antenna Theory : Analysis and Design*, 3rd ed., John Wiley & Sons, Hoboken, New Jersey, 2005 2. John D.Kraus, Ronald J.Marhefka "*Antennas: for all Applications*" 4th ed., Tata McGraw-Hill Inc., New Delhi, 2006. **Reference Books:** 1. E C Jordan and K G Balmain, *Electromagnetic Waves & Radiating Systems*, 2nd ed., Pearson, New Delhi, 2015 2. R. C. Johnson and H. Jasik, "*Antenna Engineering handbook*", 3rd ed., Mc-Graw Hill Inc., New York, 1993. 3. I. J. Bhal and P. Bhartia, "Micro-strip antennas", Artech house, Dedgham, MA, 1980. 4. Online Reference Material(s): 1. https://nptel.ac.in/courses/117107035/

MT/EC9038: Antenna Analysis & Synthesis [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	Ability to characterize resonance and radiation property of an antenna based on application.	**2**	**1**	**2**	**2**	**3**	**1**
CO2	Learn various design parameters that affects an antenna and antenna array patterns.	**3**	**2**	**3**	**2**	**1**	**2**
CO3	Understand different types of antenna based on the radiation mechanism like wire antenna, aperture antennas, traveling wave antenna.	**2**	**1**	**3**	**1**	**2**	**1**
CO4	Understand different types of antenna based on the design mechanism like log periodic antenna, log spiral antenna and electrically long antenna as well as electrically small antenna.	**3**	**2**	**3**	**2**	**2**	**2**
CO5	Design suitable antenna feeding mechanism as well as matching mechanism.	**2**	**2**	**3**	**2**	**3**	**2**
CO6	Analyze and synthesize different types of antennas for different wireless	**3**	**2**	**3**	**1**	**2**	**2**
Average		**2.5**	**1.67**	**2.83**	**1.67**	**2.17**	**1.67**

Department of Electronics & Communication Engineering							
Course Code	**Title of the course**	Program Core (PCR) / Electives (PEL)	**Total contact hours: 57**				Credit
			Lecture (L)	Tutorial (T)	Practical (P)	Total Hours	
MT/EC9039	**Satellite Communication**	PEL	3	1	0	4	4

Course Outcomes	• **CO1:** To compute the satellite orbit parameters, design orbits and can be able to classify them based on Kepler's six elements. • **CO2:** Understand the concept of satellite launching and positioning of satellites in orbits. • **CO3:** Can do computations of link design and classify different losses in propagation for space communication. • **CO4:** Assimilate the concept of multiple accessing technique in satellite communication. • **CO5:** Develop ability to classify different types of application of satellite communication.
Topics Covered	**Module I. [L – 5; T - 1]** Historical background, Basic concepts, Frequency allocation for satellite services, orbital & spacecraft problems, comparison of networks and services, modulation techniques used for satellite communication. Spectrum Management **Module II. [L – 9; T - 3]** Orbits- Two body problem, orbital mechanics, geostationary orbit, change in longitude, orbital manoeuvres, orbital transfer, and orbital perturbations. Launch Vehicles- principles of Rocket propulsion, powered flight, Launch vehicles for communication satellite **Module III. [L – 9; T - 3]** RF link- noise, the basic RF link, satellite links (up and down) , optimization RF link, inter satellite link, noise temperature, Antenna temperature, overall system temperature, propagation factors, rain attenuation model. Tropospheric and Ionospheric effect. **Module IV. [L – 8; T - 2]** Satellite subsystems and satellite link design- Altitude and orbit control (AOC) Subsystem, TT&C, power system, spacecraft antenna, transponder, Friis transmission equation, G/T ratio of earth station. **Module V. [L – 8; T - 3]** Multiple access- FDMA, TDMA, CDMA techniques, comparison of multiple access techniques, error connecting codes. **Module VI. [L – 6; T - 2]** Application of satellite in remote sensing and surveillance; Basic of remote sensing, Electromagnetic Radiation principles, Atmospheric window, Indian satellite sensing satellite system, Active, Passive, ground based and space based remote sensing. **Total Contact Hours: (L=42, T=14)= 57**

Text Books, and/or Reference Material	**Text Books** 1. Dennis Roddy, *Satellite Communication*, 4/e, McGraw Hill, 2001. 2. Louis J. Ippolito, Jr. "*Satellite Communications Systems Engineering: Atmospheric Effects, Satellite Link Design and System Performance",* Second Edition, 2014. **Reference Books** 1. Recommendation ITU-R P.618-11, P Series Radio Wave Propagation. 2. Pratt and Bostian, *Satellite Communication*, 2/e, John Wiley and Sons, 2000. 3. Floyd F. Sabins, *Remote Sensing: Principles and Interpretation*, 3rd edition (August 1996), W H Freeman & Co, 1996. 4. Tri T Ha, *Digital Satellite Communication*, McGraw Hill, 2001.

MT/EC9039: Satellite Communication (Elective)
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	To compute the satellite orbit parameters, design orbits and can be able to classify them based on Kepler's six elements.	1	1	2	2	3	1
CO2	Understand the concept of satellite launching and positioning of satellites in orbits	3	2	3	2	1	2
CO3	Can do computations of link design and classify different losses in propagation for space communication.	2	1	3	1	2	1
CO4	Assimilate the concept of multiple accessing techniques in satellite communication.	2	2	3	2	2	2
CO5	Develop ability to classify different types of application of satellite communication.	1	3	2	2	1	3
Average		1.8	1.8	2.6	1.8	1.8	1.8

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total contact hours: 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9040</td><td>Artificial Intelligence and Soft Computing</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">• CO1: Basics of optimization and soft computing algorithms
• CO2: Learn different soft computing algorithms
• CO3: Learn artificial neural network and its training
• CO4: Study of radial basis function neural and its training
• CO5: Study of machine learning algorithms and clustering</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction to Optimization and soft computing algorithms [L – 8; T - 3]
Introduction to optimization, Constrained and unconstrained optimization, Introduction to Optimization based on soft computing, Genetic algorithms, Quantum particle swarm optimization, Whale optimization, Crow search algorithm.

Module II. Review of different soft computing algorithms part-I [L – 7; T - 2]
Flower pollination algorithm, Teaching learning based optimization, Sine cosine algorithm, Moth flame optimization.

Module III. Review of different soft computing algorithms part-II [L – 5; T - 2]
Backtracking search optimization Algorithm, Particle swarm optimization, Firefly algorithm

Module IV. Basics of artificial neural network and its training [L – 7; T - 2]
Introduction to artificial neural network, Supervised Learning Neural Networks, Perceptrons, Adaline, Multilayer feed forward neural network, Training of neural network using back propagation algorithm, Training of neural network using soft computing technique

Module V. Radial basis function neural networks and K-means clustering[L – 5; T - 2]
Radial Basis Function Neural Networks (RBF), Training of RBF using pseudo inverse technique ,Data clustering using K-means

Module VI. Study of machine learning algorithms[L – 10; T - 3]
Extreme learning machine (ELM), Kernel based ELM, Random vector functional link neural network (RVFL), Training and testing of ELM and RVFL,CNN.
Total Contact Hours: (L=42, T=14)= 56</td></tr>
<tr><td>Text Books, and/or Reference Material</td><td colspan="7">Text Books:
1. S N Sivanandam, S. N. Deepa, “Principles of Soft Computing,” Wiley,3rd edition,2018
2. Samir Roy & Udit Chakraborty, “Introduction to Soft Computing,” Pearson,1st edition,2013
3. Satish Kumar, “Neural Networks: A Classroom Approach”, McGraw-Hill (India), 2013
4. Shai Shalev-Shwartz and Shai Ben-David, “Understanding Machine Learning: From Theory to Algorithms,” Cambridge University Press,2014
Reference Books:
1. S. Rajasekaran and G.A.V. Pai, “Neural Networks, Fuzzy Logic and Genetic Algorithms”, PHI,2003
2. Jang, Sun, Mizutani, “Neuro-Fuzzy and Soft computing”, Pearson, 2015
3. Simon Haykin, “Neural networks and learning machines”, Pearson, 3rd edition, 2009
4. Charu C.Aggarwal, “Neural Networks and Deep learning”, Springer, 2018</td></tr>
</table>

MT/EC9040: Artificial Intelligence and Soft Computing (Elective) [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	Basics of optimization and soft computing algorithms.	2	2	3	1	1	3
CO 2	Learn different soft computing algorithms.	3	2	2	1	1	3
CO 3	Learn artificial neural network and its training.	2	2	2	1	1	3
CO 4	Study of radial basis function neural and its training.	3	2	3	1	1	3
CO 5	Study of machine learning algorithms and clustering.	2	2	2	1	1	3
Average		**2.4**	**2.0**	**2.4**	**1.0**	**1.0**	**3.0**

Department of Electronics and Communication Engineering							
Course Code	Title of the course	Program Core (PCR) / Electives (PEL)	Total contact hours: 57				Credit
			Lecture (L)	Tutorial (T)	Practical (P)	Total Hours	
MT/EC9041	**RF IC Design**	PEL (Open Elective)	3	1	0	4	4

Course Outcomes	After going through the course, student will be able to • **CO1:** Analyze various architectures of today's digital radio transmitters and receivers. • **CO2:** Analyze and design basic RF building-blocks in CMOS technology. • **CO3:** Define basic RF measurements parameters such as S-parameters, sensitivity, noise figure, IIP3 • **CO4:** Assimilate the design techniques VCO, LNA as well as other front-end circuits
Topics Covered/ Syllabus	**Module-I: Introduction to RF IC Design Concepts [L – 6; T – 2]** Basic Concepts in RF Design, passive on chip components and layouts, transceiver architectures, circuit analysis techniques at radio frequencies. **Module-II: Semiconductor radio frequency components [L – 8; T – 3]** RF diodes, MOS transistor, determination of model parameters, parasitics of MOS transistors and high frequency behaviour of basic amplifier. RF Transistor Materials – The Transistor Equivalent Circuit – Y Parameters – S Parameters – Understanding RF Transistor Data Sheets; BSIM3 parameters of NMOS and PMOS transistors, matching and biasing networks for transistors **Module-III: Noise and non-linearity. [L – 3; T – 1]** Noise Figure and representation of non-linearity, intermodulation products and intercept points **Module-IV: Filter Design [L – 4; T – 1]** Resonator and filter configurations, realization of filter for specific transfer function, implementation of filters a coupled line filter. **Module V:RF Transistor Amplifier[L – 8; T – 3]** Stability consideration, constant, gain and noise figure circles. Low Noise Amplifiers: SNR, LNA topologies, power constrained CMOS LNA design, low-current CMOS inverter LNAs, low-voltage LNA topologies, differential LNA design methodology, process variation in tuned LNAs, impact of temperature variation in tuned LNAs, low-noise bias networks for LNAs, MOSFET layout of LNA. **Module-VI: RF Mixers [L – 5; T – 1]** Basic design concepts, single end diode mixer single balanced and double balanced diode mixer design. Transistor mixers, conversion loss. **Module-VII: RF Oscillators [L – 6; T – 2]** Basic Principles, Phase Noise, negative resistance oscillators, transistor oscillators, VCO design methodology, frequency scaling of CMOS VCO, VCO layout Phase lock loops, frequency synthesizers

	Module-VIII:RF power amplifiers [L – 3; T – 1] Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations **Total Contact Hours: (L=43, T=14)= 57**
Text Books, and/or Reference Materials	**Text Books:** 1. Behzad Razavi, "*RF Microelectronics*", Prentice Hall of India, 2001 2. Sorin Voinigescu, "*High Frequency Integrated Circuits*", Cambridge University Press,UK, 2013 **Reference Books:** 3. Thomas H. Lee, "*The Design of CMOS Radio Frequency Integrated Circuits*", Cambridge University Press. 4. R Ludwig and P Bretchko, "*RF Circuit Design: Theory and Application*", Pearson Education, New Delhi 5. Bosco Leung, "*VLSI for Wireless Communication*", Springer (2011). 6. Ivan Chee-Hong Lai, Minoru Fujishima, "*Design and Modeling of Millimeter-wave CMOS Circuits for Wireless Transceivers*", Springer Netherlands,2008

MT/EC9041: RF IC Design (Elective)
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Analyze various architectures of today's digital radio transmitters and receivers	2	1	2	2	1	1
CO 2	Analyze and design basic RF building-blocks in CMOS technology	3	1	3	3	3	1
CO 3	Define basic RF measurements parameters such as S-parameters, sensitivity, noise figure, IIP3	3	2	3	2	2	1
CO 4	Define basic RF measurements parameters such as S-parameters, sensitivity, noise figure, IIP3	3	2	3	2	2	1
CO 5	CO#4:Assimilat the design techniques VCO, LNA as well as other front end circuits	2	1	2	3	3	2
Average		**2.50**	**1.33**	**2.50**	**2.67**	**2.50**	**1.33**

Department of Electronics and Communication Engineering							
Course Code	Title of the course	Program Core (PCR) / Electives (PEL)	Total contact hours: 56				Credit
			Lecture (L)	Tutorial (T)	Practical (P)	Total Hours	
MT/EC9042	**SoC Design**	PCR (Program Core)	3	1	0	4	4

Course Outcomes **After going through the course, student will be able to**	On successful completion of this course, students should have the skills and knowledge to: • **CO1:** Knowledge and understanding of: ○ Arm processor architectures and Arm-based SoCs ○ Capture the design of Arm-based SoCs in a standard hardware description language ○ Low-level software design for Arm-based SoCs and high-level application development • **CO2:** Intellectual ○ Ability to use and choose between different techniques for digital system design and capture; ○ Ability to evaluate implementation results (e.g. speed, area, power) and correlate them with the corresponding high level design and capture; • **CO3:** Practical ○ Ability to use a commercial tools to develop Arm-based SoCs
Topics Covered/ Syllabus	**Module I. Design and Technology Trends [L – 1, T -0]** Introduction to design trends in deep-submicron (DSM) era, including scaling trend, clock cycle and power issues. **Module II. Role of Interconnect in Contemporary SoC Design [L – 2, T -0]** Characteristics of wire delay in DSM, crosstalk minimization, delay in long wire and performance limitations, interconnect coupling capacitance and its effect on wire delay, crosstalk avoidance coding schemes (CAC), fault modeling in presence of crosstalk, interconnect inductance. **Module III. System-on-Chip and Platform based Design [L – 2, T -0]** Emerging SoC trends: IP based design and reusability, multiprocessor SoC platform design, design for testability (DFT), Test Access Mechanism (TAM), concepts of core based test and IEEE P1500 standard for SoC test. **Module IV. Importance of Power and Low Power SoC Design Methodology [L – 2, T -0]** Different low power design methodologies, physics of power dissipation in CMOS, design and test of low-voltage CMOS circuits, multi-threshold CMOS (MTCMOS), variable threshold CMOS and other related methodologies, coding for low power, power dissipation through architecture level optimization. **Module V. ARM based SoC: [L – 2, T -0]** Introduction to Programmable SoCs; Why the SoC Design Concept Developed, Moore's Law, Why Scaling?, The Design Productivity Gap, Bridging the Design Productivity Gap, What Is an SoC?, What Is Inside an SoC?, Example Arm-based SoC, Advantages of SoCs, Limitations of SoCs, SoC

v Microcontroller v Processor, SoC Design Flow, SoC Example: NVIDIA Tegra 2, SoC Example: Apple SoC Families.

Module VI. The Arm Cortex-M0 Processor Architecture: Part 1[L – 3, T -1]
Building a System on a Chip, Arm Holdings, What Is Arm Architecture?, Example Design of an Arm-based SoC, Arm Processor Families, Arm Cortex-M Series Family, Cortex-M0 Processor, Arm Processor v Arm Architectures, Cortex-M0 Overview, Cortex-M0 Block Diagram, Cortex-M0 Three-stage Pipeline, Cortex-M0 Block Diagram, Cortex-M0 Registers, Cortex-M0 LR, Cortex-M0 PSRs, Cortex-M0 Memory Map, Cortex-M0 Executable Memory Space, Cortex-M0 Device Memory Space, Cortex-M0 Private Peripheral Bus, Cortex-M0 Reserved Memory Space, Cortex-M0 Memory Map Example, Cortex-M0 Endianness

Module VII. The ARM Cortex-M0 Processor Architecture part-2 [L – 3, T -1]
Building a System on a Chip, Thumb Instruction Set, Thumb-2 Instruction Set, Cortex-M0 Instruction Set, Cortex-M0: Generic Format of Instructions, Cortex-M0 Instruction Set, Register Access: The Move Instruction, Memory Access: The LOAD Instruction, Memory Access: LOAD, Memory Access: The STORE Instruction, Memory Access: STORE, Multiple Data Access, Stack Access: PUSH and POP, Arithmetic ADD, Arithmetic SUB, MUL, Arithmetic CMP, Logic Operation, Arithmetic Shift Operation, Logical Shift Operation, Rotate Operation, Reverse Ordering Operation, Extend Operation, Program Flow Control, Suffixes for Conditional Branch (B <cond>), Conditional Branch Example, Memory Barrier Instructions, Exception-Related Instructions, Other Instructions, Sleep Mode Related Instructions, Low-Power Requirements, Cortex-M0 Low Power Features, Cortex-M0 Sleep Mode, Sleep-on-Exit Feature, How to Enable Sleep Features, Processor Wakeup Conditions, Wakeup Interrupt Controller, Enter and Exit Deep Sleep Mode, Developing Low-Power Applications

Module VIII. The AMBA3 AHB Lite Bus Architecture [L – 3, T -1]
Building a System on a Chip, What Is a Bus?, Bus Terminology, Bus Operation in General, A Typical Bus Operation Example, Communication Architecture Standards, Arm AMBA System Bus, Arm AMBA Bus Families, AMBA 3 AHB-Lite Bus, AHB-Lite Bus Block Diagram, AHB-Lite Master Interface, AHB-Lite Slave Interface, Address Decoder, Slave Multiplexor, Hardware Implementation, AHB-Lite Operation Principles, AHB-Lite Bus Timing, Basic Read Transfer, Basic Write Transfer, Read Transfer with Wait State.

Module IX. ARM AHB Bus Peripherals: [L – 2, T -1]
Design and Implementation of an AHB VGA Peripheral: Building a System on a Chip, VGA Overview, How VGA Signals Work, VGA Timing, AHB VGA Peripheral, Additional Design Requirement, AHB VGA Peripheral Hardware Architecture, VGA Interface, VGA Image Buffer, Text Console, AHB Interface, Memory Space.

Module X. Design and Implementation of an AHB UART peripheral [L – 2, T -1]
Building a System on a Chip (SoC), Serial Communication, Types of Serial Communication, Parallel Communication, Serial v Parallel Communication, UART Overview, UART Protocol, Character-Encoding Scheme, ASCII Encoded Characters, AHB UART Peripheral, Baud Rate Generator, UART Transmitter, UART Receiver, First In First Out (FIFO), Why Do We Need an FIFO in UART?, First In First Out (FIFO), FIFO Implementation, Memory Space

Module XI. Design and Implementation of an AHB timer, a GPIO peripheral, and a 7-segment display peripheral [L – 2, T -1]
Building a System on a Chip (SoC), Timer Overview, Standard Architecture of Hardware Timers, Timer Operation Modes, Timer Operation Mode, Timer Operation Modes, Hardware Module Overview, AHB Timer, Timer Registers, Hardware Module Overview, GPIO Overview, AHB GPIO, GPIO Registers, Hardware Module Overview, 7-Segment Display Overview, AHB 7-Segment Display, 7-Segment Display Registers, Memory Space.

Module XII. Design and Implementation of Interrupt Mechanism [L – 2, T -1]

	Building a System on a Chip (SoC), Polling v Interrupts, Exception and Interruption, Interrupt Preemption, Cortex-M0 Block Diagram, Armv6-M Exception Model, Cortex-M0 Interrupt Controller, NVIC Registers, NVIC Registers, Building a System on a Chip (SoC), The Interrupt Mechanism Process, Interrupt Implementation for Timer, Interrupt Implementation for UART, Connect Interrupts to Processor, Enable Interrupts in Software, Entering an Exception Handler, Exiting an Exception Handler. **Module XIII. Software Programming of ARM SoC: [L – 2, T -1]** Programming an SoC Using C Language; Building a System on a Chip (SoC), C and Assembly Language Review, Typical Program-Generation Flow, Program-Generation Flow with Arm Tools, Program Image, Program Image in Global Memory, Program Data Types, Data Qualifiers in C Language, How Is Data Stored in RAM, Example of Data Storage, Define Interrupt Vector in C, Define Stack and Heap, Accessing Peripherals in C, Calling a C Function from Assembly, Calling an Assembly Function from C, Embedded Assembly **Module XIV. ARM CMSIS and Software Drivers [L – 2, T -1]** Building a System on a Chip (SoC), What Is CMSIS?, What Is Standardized in CMSIS?, CMSIS Components, Access NVIC Using CMSIS, Access Special Registers Using CMSIS, Execute Special Instructions Using CMSIS, Access System Using CMSIS, Benefits of CMSIS, Device Driver, AHB Peripheral Drivers, Using Pointer to Access Peripherals, Define Data Structure for Peripherals, Functions Reuse Between Multiple Units, Define AHB Peripherals, Examples of Simple Functions **Module XV. Application Programming Interface (API) and Final Application: The SNAKE Game [L – 3, T -1]** Building a System on a Chip (SoC), API Overview, Develop a Simple API, Hardware-Dependent Functions, Call-Back Functions, Retargeting, Retargeting Examples, Example of API Functions, Game Application: Snake, More Game Applications, Cortex-M0 Low-Power Features Review, Cortex-M0 Sleep Mode, System Control Register, Sleep-on-Exit, Polling v Interrupts, Developing Low-Power Applications. **Module XVI. ARM DS-5 Development Studio [L –3, T -1]** Arm DS-5 Development Studio Overview, ARM DS-5 Code, ARM DS-5 Build, ARM DS-5 Debug, Debug Hardware, Virtual Debug Interface – VSTREAM, ARM DS-5 Analyzer – Streamline, ARM DS-5 Analyzer – Energy Probe, ARM DS-5 Simulation, ARM DS-5 Device Configuration Database **Module XVII. ARM v7-A/R ISA [L – 2, T -1]** Why do u need to know Assembler?, ARM assembler file syntax, Single/ Double register data transfer, Addressing Memory, Pre- and Post -Indexed Addressing, Multiple Register Data Transfer, Data Processing Instructions, Shift/Rotate Operations, Instructions for loading constants, Multiply/Divide, Bit Manipulation Instructions, Byte Reversal, Flow control, Branch instructions, Interworking, Compare and Branch if zero, Conditional Instructions, If Then, Coprocessor instructions, PSR access, DSP instructions overview, Saturated Maths and CLZ, Saturation, SIMD **Module XVIII. ARM Cortex-A9 Processor [L – 2, T -1]** Cortex- A9, Cortex-A9 MP Core, Cortex-A9 MPE Configuration, Cortex-A9 Media Processing Engine, Register Renaming, Virtual Flags Registers, Small Loop Mode, Program Flow Prediction, Performance Monitoring Unit (PMU), Cortex A9 supports ARMv7-A Architecture, caches, Data Cache, Memory Management Unit, ARM v7 Architecture Effects. **Module XIX. AMBA AXI4 Bus Architecture [L – 2, T -1]** What is a Bus, Bus Types, Bus Terminology, Bus Operation, Communication Architecture Standards, ARM AMBA System Bus, AMBA 3 AXI Interface, AMBA 4 Specifications, AXI Components and Topology, Transcation Channels, Basic Signals, Clock and Reset, Channel Timing Example, Relationship between the Channels. **Total Contact Hours: (L=42, T=14)= 56**

Text Books, and/or Reference Materials	**Text Books:** 1. Steve B. Furber, ARM System-on-Chip Architecture. 2. William Hohl, ARM Assembly Language: Fundamentals and Techniques. 3. Joseph Yiu, The Definitive Guide to the ARM Cortex-M0.
	Reference Books/Materials: 1. Cortex-A Series Programmer's Guide for ARMv7-A by Arm 2. http://infocenter.arm.com/help/topic/com.arm.doc.den0013d/index.html 3. Louise H Crockett, Ross A Elliot, Martin A Enderwitz, The Zynq Book Tutorials for Zybo and ZedBoard

MT/EC9042: SoC Design (Elective) **[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]**							
CO	**Statement**	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	**Knowledge and understanding of:** Arm processor architectures and Arm-based SoCs Capture the design of Arm-based SoCs in a standard hardware description language, Low-level software design for Arm-based SoCs and high-level application development	2	3	2	3	2	3
CO 2	**Intellectual:** Ability to use and choose between different techniques for digital system design and capture; Ability to evaluate implementation results (e.g. speed, area, power) and correlate them with the corresponding high level design and capture;	3	3	3	3	2	3
CO 3	**Practical:** Ability to use a commercial tool to develop Arm-based SoCs	3	3	3	3	3	3
Average		**2.66**	**3**	**2.66**	**2.5**	**2.33**	**3**

<table>
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<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total contact hours: 70 (L-42 + P-28)</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9043</td><td>FPGA based Design</td><td>PEL</td><td>3</td><td>0</td><td>2</td><td>5</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">• CO1: Learn logic synthesis techniques – two level and multilevel synthesis.
• CO2: Be able to design systems using FPGAs and CPLDs.
• CO3: Learn sequential machine design using FPGAs.
• CO4: Learn to design systems for low power operation.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: Lecture – 42; Practical/Sessional – 28: Total Contact Hours – 70

Module-I: (L – 06)
Logic design fundamentals: Two level synthesis – SOP/POS forms, Logic minimization, Limitations of two-level synthesis, introduction to multi-level synthesis.

Module-II: (L – 10)
Programmable Logic Devices: Programmable Logic Array (PLA) architecture; Programmable Array Logic (PAL), PAL vs. PROM, Fan-in expansion feature, Architecture for sequential circuit implementation, Typical PAL chips; Complex Programmable Logic Devices (CPLD).

Module-III: (L – 10)
Programmable Gate Arrays: Gate Array concept, Mask programmable and Field Programmable Gate Arrays; Look up tables (LUT) Configurable logic blocks (CLB), logic design using LUT’s; Multi-level synthesis techniques – Factoring and Functional decomposition, Shannon’s Expansion Theorem; Generalized FPGA Architecture; Introduction to CAD Tools for FPGA based design, design entry and simulation – introduction to HDL, synthesis, post synthesis simulation, interfacing external devices.

Module-IV: (L – 08)
Sequential Circuit Design: Finite State Machines, Moore and Mealy Machines; State diagrams, State table, State assignment, derivation of next-state and output expressions, state minimization; State assignment for low power operation; CAD tools for FSM synthesis; Designing a simple CPU, concept of embedded system.

Module-V: (L – 02)
Advanced features of modern FPGAs: Block RAMs, Embedded processor, Communication ports, Analog interface.

Module-VI: (L – 06)

FPGA as a Hardware Debugging platform: Hardware troubleshooting methods, Looking into the chip – Logic State Analyzer and its use; Concept of Hardware emulation – simulation vs. Emulation, FPGA as a Hardware emulator, Break-points and their utility, setting break-points in FPGA based design.

Module-VII: (P – 18)
Familiarizing with CAD tools, Design and synthesis of simple logic functions – Basic gates, adder/subtractor, decoder, encoder, multiplexer, demultiplexer; Interfacing external devices – setting user constraint file, interfacing input (switch) and output (LED) devices, BCD to seven-segment decoder, keyboard/display interface; designing memory elements and arrays; sequential machine</td></tr>
</table>

	design – sequence generators, timing generators, a typical machine design (example: vending machine); A simple CPU design, constructing a basic embedded system – interfacing on-chip CPU, memory and I/O ports. **Module-VIII:** (P – 10) Design analysis: Static timing analysis, Power analysis, Resource utilization, noise, clock network, DRC, debugging methods. **Total Contact Hours: (L=42, P=28) = 70**
Text Books, and/or Reference Materials	Text Books: 1. S. Brown and Z. Vranesic, "*Fundamentals of Digital Logic with Verilog Design*," McGraw Hill Education Special India Edition (SIE), 2017. Reference Books: 1. J. Bhasker, "*A Verilog HDL Primer*", B.S. Publications, Hyderabad in arrangement with Star Galaxy Publishing, USA, 1999.

MT/EC9043: FPGA based Design (Elective)
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Learn logic synthesis techniques – two level and multilevel synthesis.	2	1	2	2	1	1
CO 2	Be able to design systems using FPGAs and CPLDs.	3	1	3	3	3	1
CO 3	Learn sequential machine design using FPGAs.	3	2	3	3	3	1
CO 4	Learn to design systems for low power operation.	3	2	3	2	2	1
Average		**2.75**	**1.5**	**2.75**	**2.5**	**2.25**	**1**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9044</td><td>MEMS & Microsystems Technology</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course the student will be able to
• CO 1: Understand characteristics of MEMS system
• CO 2: Understand fundamental building blocks of general MEMS systems
• CO 3: Apply qualitative and quantitative analysis techniques in general MEMS systems
• CO 4: Understand fabrication technology of MEMS system
• CO 5: Investigate application specific MEMS systems</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I: Introduction to MEMS & Microsystems Technology [L1]
History of MEMS technology, Commercial MEMS devices, Application of MEMS devices

Module II: Electromechanical transduction techniques [L-5; T-2]
Electrostatic transduction, Electromagnetic transduction, Piezoelectric transduction, Piezoresistive transduction

Module III: Characteristics of MEMS Devices [L-6; T-2]
Static characteristics, linearity, nonlinearity, Sensitivity, Resolution, Hysteresis, Dynamic characteristics, Response time, Delay time, Gain, Bandwidth, Quasi static characteristics of MEMS devices.

Module IV: Analysis and Modelling of MEMS devices [L-6; T-2]
Concept of Energy, Co-energy, Energy methods, Lagrange equations, Physics based model, Lumped model, Finite element model

Module V: Effect of noise [L-2; T-1]
Sources of different types of noise, Thermal noise, Environmental noise, Noise modelling techniques, Statistical methods of noise modelling

Module VI: Integration and packaging [L-6; T-3]
Transducers in MEMS, MEMS sensors, MEMS actuators, Integration of MEMS transducers with signal conditioning /driver circuits, Signal amplifiers, Signal filters

Module VII: MEMS device fabrication processes [L-10; T-2]
MEMS materials, Bulk micromachining, Silicon anisotropic etching, Surface micromachining,

Module VIII: Scaling effect, Reliability of MEMS devices [L-2; T-1]
Effect of inertia in MEMS devices, Scaling effect of MEMS devices, Concept of reliability, Mathematical modelling of reliability, Reliability analysis of MEMS devices.

Module IX: Case studies in MEMS [L-4; T-1]
Application specific MEMS devices, MEMS blood pressure sensors, MEMS microphone, MEMS accelerometer, MEMS gyro

Total Lecture Hours: (L=42, T=14)= 56</td></tr>
</table>

Text Books, and/or reference material	**Text Books:** 1. S. D. Senturia, *Microsystem Design*, Springer; 1st edition, 2004 2. K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat, V.K. Aatre, G.K. Ananthasuresh, *Micro and Smart Systems*, Wiley India Pvt Ltd, 2010 **Reference books:** 1. Research Articles

MT/EC9044: MEMS & Microsystems Technology (Elective) [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**	
CO 1	Understand characteristics of MEMS system	2	3	2	3	1	
CO 2	Understand fundamental building blocks of general MEMS systems	3	3	2	3	1	2
CO 3	Apply qualitative and quantitative analysis techniques in general MEMS systems	3	3	3	3	1	1
CO 4	Understand fabrication technology of MEMS system	2	3	2	3	1	2
CO 5	Investigate application specific MEMS systems	3	3	2	3	1	
Average		**2.6**	**3**	**2.2**	**3**	**1**	

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9045</td><td>Embedded Systems</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course the student will be able to

• CO 1: Understand use of Microprocessor in Microcontrollers and Microcomputer
• CO 2: Interface I/O devices with Microprocessor in Microcontrollers and Microcomputer
• CO 3: Design software controlled hardware systems
• CO 4: Investigate application specific embedded systems</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I: Intel 8051 Microcontroller [L-4;]
Architecture of Intel 8051 Microcontroller using functional blocks, Crystal oscillators, Digital I/O Pins, Digital I/O ports, 8051 Microcontroller programmer, limitations of Intel 8051 Microcontroller.

Module II: ATmega Microcontrollers and Arduino [L-4;]
Architecture of ATmega Microcontrollers using functional blocks, Hardware components of Arduino boards, ADC, Analog input pins, Digital I/O pins, PWM signals, PWM pins, Serial communication pins, Arduino shields, Limitations of ATmega Microcontrollers and Arduino.

Module III: Raspberry Pi Micro-Computer [L-4]
ARM processor, Hardware components of Raspberry Pi Micro-computer, GPIO pins in Raspberry Pi board, PWM signals, Raspberry Pi OS, In-built data communication devices, Limitations of Raspberry Pi Micro-Computer.

Module IV: I/O devices for Micro controllers and Microcomputers [L-5; T-2]
Sensors, Resistive sensors, Capacitive sensors, Inductive sensors, Actuators, Motors, Signal conditioning circuits, Amplifiers, Filters, Display elements, Data storage devices, Compatibility of several transducers with Intel 8051 Microcontroller, ATmega Microcontrollers and Arduino, Raspberry Pi Micro-Computer

Module V: Embedded System Programming using Keil [L-7; T-3]
Keil editor and compiler, Keil Programming for Intel 8051 Microcontroller, Program uploading to 8051 Microcontroller, I/O programming, Interfacing Analog and Digital sensors and actuators with Intel 8051 Microcontroller, Interrupt programming in 8051, Keypad and Display element interfacing with 8051.

Module VI: Embedded System Programming using Arduino language [L-7; T-3]
Arduino editor and compiler, Arduino Programming, Program uploading to Arduino board, I/O programming, Interfacing Analog and Digital sensors and actuators with Arduino, Serial communication and Data transmission in Arduino, Interrupt programming in Arduino, Keypad and Display element interfacing with Arduino.

Module VII: Embedded System Programming using Python [L-7; T-3]
Raspberry Pi OS, Python programming, Interfacing Analog and Digital sensors and actuators with Raspberry Pi, I/O programming in Raspberry Pi, Serial communication and Data transmission in Raspberry Pi, Interrupt programming, Keypad and Display element interfacing with Raspberry Pi.</td></tr>
</table>

	Module VIII: Case studies **[L-4; T-3]** Application specific embedded system design using 8051 Microcontroller, Arduino, Raspberry Pi, Password lock device using Embedded system, Smart home using embedded system, Motor controller using Embedded system **Total Lecture Hours: (L=42, T=14)= 56**
Text Books, and/or reference material	**Text Books:** 1. T. Givargis, F. Vahid , *Embedded System Design: A Unified Hardware / Software Introduction*, Wiley; Student edition, 2006 2. E. A. Lee, S. A. Seshia, *Introduction to Embedded Systems - a Cyber Physical Systems Approach*, PHI Learning Pvt Ltd, MIT Press; Second edition, 2019 3. M. A. Mazidi, *The 8051 Microcontroller and Embedded Systems: Using Assembly and C*, Pearson Education India; 2nd edition, 2007 **Reference books:** 1. J. Bentley, *Principles of measurement systems*. Pearson Education India; 3rd edition, 2002 2. T. W. Schultz, *C and the 8051, Vol.I: Hardware, Modular Programming & Multitasking*, Prentice Hall; 2nd edition, 1997 3. S. Monk, *Programming Arduino: Getting Started with Sketches*, Second Edition, McGraw-Hill, 2nd edition, 2016 4. J. Yiu, *The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors*, Newnes; 3rd edition, 2013 5. S. Monk, *Raspberry Pi Cookbook: Software and Hardware Problems and Solutions*, Shroff/O'Reilly; Second edition, 2016 6. D. Molloy, *Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux*, Wiley; 1st edition, 2016 7. Research Articles

MT/EC9045: Embedded Systems (Elective)
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Understand use of Microprocessor in Microcontrollers and Microcomputer	2	3	3	2	1	2
CO 2	Interface I/O devices with Microprocessor in Microcontrollers and Microcomputer	3	3	3	2	1	3
CO 3	Design software controlled hardware systems	3	3	3	2	1	3
CO 4	Investigate application specific embedded systems	2	2	2	2	1	2
Average		**2.5**	**2.75**	**2.75**	**2**	**1**	**2.5**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9046</td><td>Internet of Things (IoT)</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course the student will be able to
• CO1: Understand the concept of IoT systems
• CO2: Analyze electronic systems and IoT architecture
• CO3: Apply data analysis techniques in IoT
• CO4: Analyze case studies</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction to IoT [L-1]
Evolution of IoT, Applications of IoT in different domain.

Module II. Building Blocks of IoT [L-5; T-3]
Functional physical building blocks of IoT architecture, Sensors, Actuators, Signal conditioning elements and Data acquisition blocks, Data processing units.

Module III. Data Communication [L-4; T-2]
Data communication schemes, Basics of Networking, Communication Protocols, MQTT, HTTP, Sensor Networks, Intranet, Internet, NFC, Bluetooth, Zigbee, Wifi, 4G, 5G

Module IV. IoT System using Arduino board and Arduino programming [L-8; T-2]
Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino board, Data acquisition using Arduino board, Arduino communication shields, Data communication using Arduino-integrated-computer system.

Module V. IoT System using Arduino, Raspberry Pi and Python Programming [L-6; T-2]
Introduction to Raspberry Pi, Raspberry Pi OS and Python programming, Integration of Sensors and Actuators with Arduino and Raspberry Pi, Data acquisition using Arduino and Raspberry Pi, Integrated Sensor Network, Data communication using Raspberry Pi, Data communication using Raspberry Pi -integrated-computer system.

Module VI. Data processing [L-8; T-2]
Introduction to SDN, SDN for IoT, Introduction to Cloud Computing, Sensor-Cloud, Introduction to Fog Computing, Introduction to Edge Computing, Data analysis

Module VII. IoT applications and Case Studies [L-8; T-3]
Smart Homes, Smart Cities, Connected vehicles, Smart Grid, Industrial IoT, Smart-agriculture, Tele-medicine, Body activity monitoring

Module VIII. IoT and Industry 4.0 [L-2]
Industry standards, Scope of IoT in Industry 4.0.

Total Lecture Hours: (L=42, T=14)= 56</td></tr>
<tr><td>Text Books, and/or reference material</td><td colspan="7">Test Books:
1. E. A. Lee, S. A. Seshia, Introduction to Embedded Systems - a Cyber Physical Systems Approach, MIT Press; Second edition, 2019
2. D. Hanes, G. Salgueiro, P. Grossetete, R. Barton, J. Henry, “IoT fundamentals: Networking technologies, protocols, and use cases for the internet of things”, Pearson Education; First edition, 2017</td></tr>
</table>

3. J. Bentley, *Principles of measurement systems*. Pearson Education India; 3rd edition, 2002
4. A. Bahga and V. Madisetti. *Internet of Things: A hands-on approach*. Orient Blackswan Private Limited; First edition, 2015
4. B. A. Forouzan, *Data Communications and Networking*, McGraw Hill Education; 4th edition, 2017

Reference books:

1. S. Monk, *Programming Arduino: getting started with sketches*. McGraw-Hill Education, 2nd edition, 2016
2. F. Brown, *Python: the complete reference*, McGraw Hill Education; 4th edition, 2018
3. E. Upton, and G. Halfacree. *Raspberry Pi user guide*. Wiley, 1st edition, 2012
4. Research articles

MT/EC9046: Internet of Things (IoT) (Elective)
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO 1	PSO 2	PSO 3
CO 1	Understand the concept of IoT systems	2	3	1	2	1	3
CO 2	Analyze electronic systems and IoT architecture	3	3	2	2	1	3
CO 3	Apply data analysis techniques in IoT	2	3	3	2	1	1
CO 4	Analyze case studies	3	3	3	1	1	3
Average		**2.5**	**3**	**2.25**	**1.75**	**1**	**2.5**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9047</td><td>Nanoelectronics</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">• CO 1: Demonstrate understanding of fundamental of nanodevices fabrication techniques.
• CO 2: Demonstrate understanding of nanotechnology concepts for device fabrication and characterization.
• CO 3: To acquire a fundamental understanding of electronics and optical properties of nanomaterials.
• CO 4: To acquire knowledge of basic nanodevices principles and fabrication approaches for various nanoscale devices.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction to nanotechnology [L –8; T - 2]
Introduction to nanotechnology, the size of things, history of nanotechnology, fabrication method (top-down and bottom-up), emerging applications of nanotechnology.

Module II. Electronic and optical properties of nanostructures [L – 10; T -5]
Electronic and Optical properties of nanostructures. Energy sub-bands. Electron transport in two –dimensional electron gas (density of states), Carrier scattering, the resistance of a ballistic conductor, Transmission probability calculation, Electron tunnelling, Resonant tunnelling, Coupled nanoscale structures, and Superlattices.

Module III. Nanomaterials, deposition and characterization techniques [L – 11; T - 4]
Nanotechnology: Deposition techniques for Nanoscale Devices, Nanolithography, Self-Assembly Techniques, Nanomaterials, Nanoparticles, Nanowires, Nanomagnetic Materials, Nanostructure Surfaces; Instrumentation for nanoscale electronics: The Atomic Force Microscope (AFM), Scanning Tunneling Microscope and scanning near field optical microscope.

Module IV. Electronic devices based on nanostructures [L –13; T - 3]
Shrink-down approaches: Electronic devices Based on Nanostructures: Advance Heterostructure Devices, Downscaling of the MOSFET. Nanoscale FET Transistors, the Ballistic FET, Resonant Tunneling Devices and Circuits, Single Electron Transistor and Related Devices. Devices based on carbon nanotubes, Spintronic Devices; Optoelectronic Devices using Nanostructures: Quantum well and Quantum Dot LASERS, Quantum Cascade LASER, Quantum well-infrared photodetector, Superlattice LASER.

Total Contact Hours: (L=42, T=14)= 56</td></tr>
<tr><td>Text Books and/or Reference Material</td><td colspan="7">Text Books:
1. C.P. Poole Jr., F.J. Owens, Introduction to Nanotechnology, John Wiley & Sons, Hoboken, New Jersey, 2003.
2. W.Ranier,Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices), 3rd ed., Wiley-VCH, 2003.
Reference Books:
1. J. H. Davies,The Physics of Low-Dimensional Semiconductors, Cambridge University Press, 1998.
2. Y. Taur and T. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press, 1988.
3. K. Goser, “Nanoelectronics and Nanosystems”, Springer, 2004.</td></tr>
</table>

MT/EC9047: Nanoelectronics (Elective) [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	Demonstrate understanding of fundamental of nanodevices fabrication techniques	2	1	2	2	1	1
CO 2	Demonstrate understanding of nanotechnology concepts for device fabrication and characterization.	3	1	3	3	3	1
CO 3	To quire fundamental understanding for electronics and optical properties of nanomaterials.	3	2	3	3	3	1
CO 4	To acquire knowledge of basic nanodevice principles and fabrication approaches for various nanoscale devices.	3	2	3	2	2	1
Average		**2.75**	**1.5**	**2.75**	**2.5**	**2.25**	**1**

<table>
<tr><td colspan="7">Department of Electronics & Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR)/ Elective (PEL)</td><td colspan="4">Total contact hours : 70</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td></td></tr>
<tr><td>MT/EC9048</td><td>ASIC Design using Verilog/VHDL</td><td>Elective</td><td>3</td><td>0</td><td>2</td><td></td><td>4</td></tr>
<tr><td colspan="3" rowspan="2"></td><td colspan="4"></td><td></td></tr>
<tr><td colspan="4"></td><td></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After successful completion of the course, the student will be able to:
• CO 1: Explain VLSI design flow using HDL.
• CO 2: Analyze and design combinational and sequential digital systems.
• CO 3: Employ EDA tools to model a digital system.
• CO 4: Write test benches to verify the design.
• CO 5: Compare between blocking and non-blocking statement and their uses.
• CO 6: Create a System from simulation to synthesizable design.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: Lecture – 42; Practical/Sessional – 28: Total Contact Hours – 70

Module I. Brief introduction to VLSI using CAD tools [L - 3]
Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-based design flow, Verilog HDL, Trends in HDLs.

Module-II. Hierarchical Modeling Concepts [L – 3]
Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.

Module-III. Basic Concepts [L – 3]
Lexical conventions, data types, system tasks, compiler directives.Memory modelling Logic Synthesis: Introduction synthesis of different Verilog constructs.

Module-IV. Modules and Ports [L – 3]
Module definition, port declaration, connecting ports, hierarchical name referencing.

Module-V. Gate-Level Modeling [L – 2]
Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.

Module-VI. Dataflow Modeling [L – 3]
Continuous assignments, delay specification, expressions, operators, operands, operator types.

Module-VII. Behavioural Modeling [L – 3]
Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.

Module-VIII. Tasks and Functions [L – 4]
Differences between tasks and functions, declaration, invocation, automatic tasks and functions.

Module-IX. Useful Modeling Techniques [L – 4]
Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.

Module-X. Flip-Flop and Counter Design::(L – 04) [L – 4]</td></tr>
</table>

	Synchronous and asynchronous flip flop design with set and reset, design of basic counters. **Module-XI. FSM & Processor Design:** (L – 06) **[L – 6]** FSM modeling, Data path and Controller design, Modeling Memory, Pipelining, and Design of a Processor. Introduction to Reconfigurable computing, FPGAs, the Altera /Xilinx flow. **Module-XII. Essential System Verilog for UVM** (L – 04) **[L – 4]** Overview of basic SystemVerilog, UVM verification environment: introduction to UVM methodology and universal Verification Components (UVC) structure, stimulus modeling, creating a simple environment, DUT, TLM, functional coverage modeling, register modeling in UVM. **Total Contact Hours: (L=42, P/S=28)= 70**
Text Books, and/or Reference Material	**Text Books:** 1. Samir Palnitkar, "*Verilog HDL, A Guide to Digital Design and Synthesis*", Second Edition, Pearson Education, 2004 2. J. Bhaskar, "*Verilog HDL Synthesis*", BS publications, 2001. **References:** 1. S. Brown and Z. Vranesic, Fundamentals of Digital Logic with Verilog Design, McGraw Hill, Third Edition 2013. 2. G. De Micheli. Synthesis and optimization of digital circuits, McGraw Hill, 2003 3. Indranil Sengupta, IIT Kharagpur, "*NPTEL Course on Hardware Modeling using Verilog*" (2017) https://www.youtube.com/watch?v=NCrlyaXMAn8&list=PLRsFfXmDi9IYCNlvNjrsD8bLMmNE0UxBH

MT/EC9048: ASIC Design using Verilog/VHDL (Elective)
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Explain VLSI design flow using HDL.	1	1	3	2	2	1
CO 2	Analyze and design combinational and sequential digital systems.	2	1	3	2	2	2
CO 3	Employ Verilog to model a digital system.	3	2	3	3	3	1
CO 4	Write test benches to verify the design.	3	2	3	3	3	1
CO 5	Compare between blocking and non-blocking statement and their uses.	2	1	3	3	2	2
CO 6	Create a System from simulation to synthesizable design	3	1	3	3	3	1
Average		**2.33**	**1.33**	**3**	**2.66**	**2.5**	**1.33**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9049</td><td>Mixed Signal IC Design</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">]</td><td colspan="5"></td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course, the student will be able to:
• CO 1: Explain the operation of various High performance OTAs/Opamps.
• CO 2: Design Analog Circuits using gm/ID techniques.
• CO 3: Create the Layout of a CMOS Mixed Signal System.
• CO 4: Analyze a Comparator.
• CO 5: Interpret the use of Switched Capacitor Circuits in Sampled data Systems
• CO 6: Compare Data converter architectures based on Accuracy/Area/Power/Speed.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction [L – 7; T - 2]
Overview of Mixed-Signal Design flow. Design of high performance Fully Differential Opamps: Telescopic cascode, Folded cascode, two-stage, Rail-to-Rail, Gain boosted OTAs/Opamps, Comparison.

Module II. g_m over I_D Design Process [L – 4; T - 2]
Gm over ID technique: Transconductor efficiency in sub-threshold, moderate and strong inversion. Various design plots: g_m/I_D, g_m/g_{ds}, f_T etc., and their use in Analog Design. Design of a CS Amplifier, and Two stage Opamp using g_m/I_D technique.

Module III. Opamp performance Metrics: [L – 4; T - 1]
Slew rate & Settling time, CMRR, PSRR, Linearity, Distortion: Gain Compression, THD, IIP3 calculation. Offset Cancellation techniques.

Module IV. Layout Techniques [L – 3; T - 2]
Introduction to CMOS process, CMOS Layers, Design rule basics, DRC, LVS, Passive and Transistor layout, Fingering, Inter-digitization. Matching components: Common centroid, Use of Dummy. Matching error, error propagation.

Module V. Switched Capacitor Circuits [L – 5; T - 1]
Basic philosophy of Switched capacitor circuits, design of switched-capacitor amplifiers and integrators, effect of opamp finite gain, bandwidth and offset, circuit techniques for reducing effects of opamp imperfections, switches and charge injection and clock feed-through effects.

Module VI. Sample and Hold [L – 4; T - 1]
Operation of sample and holds circuits and theirs non-idealities. Comparators: Opamp based, Strong Arm Regenerative Latch, Latch dynamics, Offset reduction.

Module VII. Data Converters [L – 12; T - 4]
Fundamentals of data converters; Introduction to data converter metrics: SNR, DNL, INL, Offset & Gain Error, SINAD, ENOB, SFDR, SDNR, Settling time etc. Nyquist rate D/A converters - voltage, current and charge mode converters, hybrid and segmented converters. Nyquist rate A/D converters (Flash, interpolating, folding flash, SAR and pipelined architectures); Oversampled</td></tr>
</table>

	A/D converters. **Module VIII. Phase Locked Loop [L – 3; T - 1]** Basic PLL topology, dynamics of simple PLL, Multiplier, phase detectors, lock acquisition, Phase frequency detector, Loop filters, Charge Pump PLLs, non-ideal effects in PLLs. **Total Contact Hours: (L=42, T=14)=56**
Text Books, and/or Reference Materialss	**Text Books:** 1. Tony Chan Carusone; David Johns; Kenneth Martin, "*Analog Integrated Circuit Design*", Wiley, 2nd Ed. 2013, 2. Behzad Razavi, "*Principles of Data Conversion System Design*", Wiley-IEEE Press, 1994 3. Adel Sedra, Kenneth Smith Tony Chan Carusone, Vincent Gaudet, "*Microelectronic Circuits*", Oxford ; 8th Ed.; 2020 **Reference Books/Materials:** 1. R. Gregorian, "*Introduction to CMOS Opamps and Comparatos*", Wiley, 1999 2. Rudy J. Van De Plassche, "*CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*", Springer, 2nd Ed. 2003. 3. Behzad Razavi, "*Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level*", Cambridge University Press, 2020.

MT/EC9049: Mixed Signal IC Design (Elective) [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	Explain the operation of various High performance OTAs/Opamps.	2	1	2	3	1	1
CO2	Design Analog Circuits using gm/ID techniques.	2	3	1	3	2	2
CO3	Create the Layout of a CMOS Mixed Signal System.	3	2	1	2	2	2
CO4	Analyze a Comparator.	3	1	1	3	2	1
CO5	Interpret the use of Switched Capacitor Circuits in Sampled data Systems	3	1	1	2	1	2
CO6	Compare Data converter architectures based on Area/Power/Speed	2	1	3	3	1	1
Average		**2.5**	**1.5**	**1.5**	**2.66**	**1.5**	**1.5**

Department of Electronics and Communication Engineering							
Course Code	Title of the course	Program Core (PCR) / Electives (PEL)	Total Number of contact hours: 56				Credit
			Lecture (L)	Tutorial (T)	Practical (P)	Total Hours	
MT/EC9050	**Low Power Circuits and Systems**	PEL	3	1	0	3	3

Course Outcomes	• **CO 1: Learn** to design and optimize CMOS logic circuits and extract parasitic elements. • **CO 2: Understand** sources of power dissipation and be able to estimate energy dissipation in typical circuits • **CO 3: Apply** different techniques to minimize dynamic dissipation. • **CO 4: Learn** the different sources of leakage in MOS transistors and how to minimize leakage dissipation at the device level as well as in circuit design.
Syllabus/ Topics Covered	**Module-I:**(L – 05: T – 02) Introduction: Need for Low power VLSI chips, MOS Transistor structure and device model, The CMOS inverter and other gates; why CMOS for Low Power? CMOS Logic design methodology, Circuit optimization for performance. **Module – II:** (L – 06; T - 02) CMOS layout and Fabrication: Typical CMOS circuit layout, IC fabrication overview, CMOS process flow, Imperfections in fabrication steps, Design rules and their importance; MOS device details – parasitic elements and their estimation, importance of device scaling. **Module – III:** (L- 06; T - 02) Power dissipation mechanisms in CMOS circuits: Static and Dynamic dissipation, Dynamic power dissipation – switching loss, short circuit dissipation, concept of switching activity; Concept of signal activity, signal probability and activity, Signal activity computation – Boolean difference, estimation of probability and activity in complex logic circuits; **Module – IV**: (L – 08, T – 03) **Dynamic dissipation management –Supply voltage scaling approaches:** Static Voltage Scaling; Single-level Voltage Scaling (SVS), Speed vs dissipation, Speed management approaches, circuit level – Transistor sizing, Architecture level – Parallel and pipeline architectures, Algorithm level transformations; Static Voltage Scaling Design Procedure, Critical path and its management; Multi-level Voltage Scaling (MVS), MVS issues – Layout, Level converters, Power up/down sequencing; Dynamic Voltage Scaling; Dynamic Voltage and Frequency Scaling (DVFS), DVFS architecture. **Module-V:** (L – 06: T - 02) **Dynamic dissipation management – Switched capacitance minimization approaches**: What is switched capacitor? Switched capacitor minimization techniques – Hardware/Software trade-off, Bus Encoding, Use of Number system, Glitching Power minimization, Architecture Level Optimization, Clock gating, State Encoding of FSM's. **Module-VI:** (L – 06: T - 02) MOS Transistor revisited: Review of quantum theory of solids, concept of quantum mechanical tunneling, Leakage mechanisms in MOS transistor – diode leakage, sub-threshold current, sub-threshold swing; short channel effects – Gate tunneling, reducing gate tunneling – high-k

	technology, DIBL and GIDL effects; Recent advances in MOS transistor design – SOI technology, FinFET, Gate All Around (GAA) FET. **Module-VII:** (L – 03; L – 01) Static Power Optimization Techniques: Comparison of static and dynamic loss in modern chips; Stand-by and Run-time leakage; Stand-by leakage reduction techniques, Transistor stacking, VT CMOS approach, Power gating, MT CMOS technology, Power gating issues, DVFS with Power gating; Run-time leakage reduction, Dynamic V_{DD} scaling, Dual V_t approach, V_t hopping. **Module-VIII:** (L – 02) Battery operated system design: Battery construction and working principle, Battery capacity and energy density, comparison of different storage cell technologies; Battery charging and discharging profiles and their effects on battery capacity and life; Design of multi-battery system installations. **Total Contact Hours: (L=42, T=14)= 56**
Text / Ref. Books	**Text Books:** 1. Ajit Pal, **"** *Low Power VLSI Circuits and Systems***"**, Springer, 2015. 2. Kaushik Roy and Sharat C Prasad, **"***Low Power CMOS VLSI circuit Design***"**, John Wiley and Sons, 2000. **References:** 1. Anantha P Chandrakasan and Robert W Brodersen, **"***Low Power Digital CMOS Design***"**, Kluwer Academic Publishers, Holland, 1995. 2. Gary B Yeap K, **"***Practical Low Power Digital VLSI Design***"**, Kluwer Academic Publishers, 1998. 3. Kuo J B and Lou J H, **"***Low Voltage CMOS VLSI Circuits***"**, John Wiley and Sons, Singapore, 1999.

MT/EC9050: Low Power Circuits and Systems (Elective) [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	**Acquire** knowledge of the fundamentals and applications of Low-power circuits	2	1	2	2	1	1
CO 2	**Identify** various leakage/ switching power sources in a MOSFET and a digital circuits.	3	1	3	3	3	1
CO 3	**Analyze the v**arious issues to power dissipation and techniques to minimize/optimize	3	2	3	3	3	1
CO 4	**Learn** various leakage/ switching power reduction mechanisms at device level and circuit level.	3	2	3	2	2	1
CO 5	**Design and implementation** of a power-aware circuits and systems	2	1	2	3	3	2
CO 6	**Evaluate** the performance of low power circuits and systems	2	1	2	3	3	2
Average		**2.50**	**1.33**	**2.50**	**2.67**	**2.50**	**1.33**

<table>
<tr><th colspan="8">Department of Electronics and Communication Engineering</th></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total contact hours: 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9051</td><td>Testing and Verification of VLSI Circuits</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>3</td><td>3</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>Course Objectives</td><td colspan="7">To expose the students, the basics of testing and verification techniques for the digital IC design.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After successful completion of the course, the student will be able to:
• CO 1: Extend knowledge of the requirement of fault modeling in VLSI circuits.
• CO 2: Generate test vectors to test a circuit efficiently covering maximum faults.
• CO 3: Demonstrate the concept of Memory testing techniques.
• CO 4: Discuss about Built-in-Self Test and its application in modern digital design.
• CO 5: Use modern tools for testing and verification.</td></tr>
<tr><td>Syllabus/
Topics Covered</td><td colspan="7">Module I. Introduction [L –4; T - 1]
Physical faults and their modeling. Fault equivalence and dominance; fault collapsing, Fault simulation: parallel, deductive and concurrent techniques; critical path tracing.

Module II. Test generation for combinational circuits[L – 4; T - 1]
Boolean difference, D-algorithm, Podem, random etc. Exhaustive, random and weighted test pattern generation; aliasing and its effect on fault coverage.

Module III. PLA testing[L – 4 T - 1]
Cross-point fault model, test generation, easily testable designs.

Module IV. Memory testing [L – 4; T - 1]
Permanent, intermittent and pattern-sensitive faults; test generation.

Module V. Delay faults and hazards [L – 6; T - 2]
Test pattern generation techniques, ATPG and its different types.

Module VI. Test pattern generation for sequential circuits[L – 6; T - 2]
Ad-hoc and structures techniques scan path and LSSD, boundary scan.

Module VII. Built-in Self-Test techniques[L – 8; T - 4]
LBIST and MBIST. Verification: logic level (combinational and sequential circuits), RTL-level (data path and control path). Verification of embedded systems. Use of formal techniques: decision diagrams, logic-based approaches.

Module VIII.ASIC/IP Verification[L – 6; T - 2]
Direct and random testing, Error detection and correction codes.

Module VIII. Post-Silicon Validation [L – 4; T - 1]
Functional test patterns development and validating, test program and test software to enable functional and tress testing of features, validation with real use case applications: OS boot and stress testing, performance validation with industry standard benchmarks, characterization of</td></tr>
</table>

	various electrical and thermal parameters as per device specification. **Total Contact Hours: (L=42, T=14)=56**
Text / Ref. Books	**Text Books:** 1. M. L. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits**", Springer, 2nd edition, 2004.** **Reference Books:** 1. A. Krstic and K-T Cheng, "*Delay Fault Testing for VLSI Circuits*", Kluwer Academic Publishers, 3rd edition,. 2003. 2. N. K. Jha and S. Gupta, "*Testing of Digital Systems*", Cambridge University Press, 2nd Edition, 2003. 3. M. Abramovici, M. A. Breuer and A. D. Friedman, "*Digital Systems Testing and Testable Design*", Wiley-IEEE Press, 3rd Edition, 1994. 4. P. K. Lala, "*Fault Tolerant and Fault Testable*", Prentice-Hall, 4th Edition, 1986.

MT/EC9051: Testing and Verification of VLSI Circuits (Elective)
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	Extend knowledge of the requirement of fault modeling in VLSI circuits.	1	1	1	2	1	1
CO 2	Generate test vectors to test a circuit efficiently covering maximum faults.	2	2	3	2	1	1
CO 3	Introduce students to the concepts Memory testing techniques.	2	2	2	3	2	1
CO 4	Understanding Built-in-Self Test and its application in modern digital design	2	2	3	2	2	1
CO 5	Use modern tools for testing and verification.	2	2	3	3	2	2
Average		**1.8**	**1.8**	**2.4**	**2.4**	**1.6**	**1.2**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9052</td><td>Computer Architecture</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3" rowspan="2"></td><td colspan="5"></td></tr>
<tr><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After successful completion of the course, the student will be able to:
• CO 1: Acquire idea about computer architecture and organization.
• CO 2: Understand the fundamental concepts of ISA.
• CO 3: Illustrate the operations of memory unit.
• CO 4: Analyze control and data flow of a computer.
• CO 5: Design and implementation of multiprocessors.
• CO 6: Evaluate the performance of a computer system.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction and Basics [L – 4; T - 1]
History of computers, introduction to computer architecture, level of transformation, abstract layers, their benefits of comfortably crossing them, instruction set architecture I, instruction set architecture II, instruction set architecture III, architecture examples, example problem and solution ideas.

Module II. Fundamental Concepts and ISA [L – 6; T - 2]
Fundamental concepts in computer architecture: Von Neumann model and data flow model, ISA principles and trade-off, elements of an ISA, RISC vs. CISC, MIPS ISA, ISA vs. microarchitecture level trade-off, property of ISA vs. microarchitecture.

Module III. Arithmetic Operations [L – 5; T - 3]
Binary arithmetic, ALU Design, multiplier design, divider design, fast addition, multiplication, floating point arithmetic.

Module IV. Processor Design [L – 8; T - 2]
Single-cycle microarchitecture, multi-cycle microarchitecture, microprogrammed microarchitecture, pipelining: issues in pipelining, data and control dependence handling, branch prediction, precise exceptions, state maintenance, state recovery; Out-of-Order execution and issues in OoO execution.

Module V. SIMD, GPUs, VLEW and DAE [L – 5; T - 1]
SIMD processing: array and vector processors, SIMD operation in modern ISAs, VLIW, Decoupled Access Execute (DAE), Systolic Array.

Module VI. Memory Hierarchy and Caches [L - 7; T - 2]
Memory hierarchy, physical memory and virtual memory, emerging memory technologies, main memory, memory controller, memory management, memory latency tolerance: prefetching, Cache organization and operation, high performance caches, memory consistency and cache coherence, in-memory processing

Module VII. Multiprocessor [L – 7; T - 3]
Multiprocessor types, multiprocessing and issues in multiprocessor, limits of parallel speedup, difficulty in parallel programming, heterogeneous systems, input/output subsystem, interfaces, I/O operations, interconnection networks: bus based and NoC based architectures.</td></tr>
</table>

	Total Contact Hours: (L=42, T=14)=56
Text Books, and/or Reference Material	**Text Books:** 1. Patterson and Hennessy, "Computer Organization and Design: The Hardware/Software Interface", 4th Edition, Morgan Kaufmann/ Elsevier, 2009. **Reference Books:** 1. Andrew Tanenbaum, "Structured Computer Organization"6th Edition, Pearson, 2016. 2. Patt and Patel, "Introduction to Computing Systems: From Bits and Gates to C and Beyond", Morgan Kaufman, Elsevier, 2th Edition, McGraw-Hill Education 2003. 3. Harvey Cragon, "Computer Architecture and Implementation", Cambridge University Press, 2000. 4. C. Hamacher, Z. Vranesic, S. Zaky, "Computer Organization", McGraw Hill Education; 5th Edition, 2011.

MT/EC9052: Computer Architecture (Elective)
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	Acquire idea about computer architecture and organization.	1	1	2	2	3	2
CO2	Understand the fundamental concepts of ISA	1	1	2	2	3	1
CO3	Illustrate the operations of memory unit	1	1	2	3	3	3
CO4	Analyze control and data flow of a computer	2	1	2	3	3	1
CO5	Design and implementation of multiprocessors.	1	1	2	3	3	3
CO6	Evaluate the performance of a computer system.	1	1	2	3	3	3
Average		**1.17**	**1**	**2**	**2.67**	**3**	**2.67**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9053</td><td>Physical System Analysis and Modeling</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="5"></td></tr>
<tr><td colspan="5"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course the student will be able to
• CO 1: Understand characteristics of physical systems
• CO 2: Apply quantitative analysis techniques to physical systems
• CO 3: Understand modeling of physical systems
• CO 4: Investigate complex designs of physical systems and case studies</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I: Introduction to physical systems [L-1]

Module II: Characteristics of Physical Elements and Systems [L-14; T-3]
Static, dynamic and quasi static characteristics of physical elements and systems, Linearity, nonlinearity, hysteresis, time domain and frequency domain characteristics, response time, delay time, frequency response.

Module III: Loading effects in two port network [L6; T-2]
Loading effects in physical systems, Loading effect modelling, Two port network representation of physical elements and systems, Lumped parameter representation of Transducer, Amplifiers, Filters.

Module IV: Error analysis and modelling [L-4; T-2]
Sources of signal errors, Systematic and Random errors, Signal error analysis, sources of noise, wide-band noise, narrow-band noise, Error modelling, Statistical methods of error measurements, statistical averages, standard deviation, Gaussian distribution, correlation, autocorrelation, regression, Static hysteresis modelling.

Module V: System Representation, Modelling, Analysis [L-13; T-4]
Bond graph representation of multiphysics system, Energy methods, Hamilton’s principle, Lagrange equations for multiphysics system, Representation of electrical circuits, electromechanical systems using Lagrange equations, Nonlinear dynamics, Time-varying Hysteresis model, Preisach model of hysteresis.

Module VI: Reliability analysis of physical systems [L-4; T-1]
Concept of reliability, mathematical modelling of reliability, bathtub model in reliability, reliability analysis of physical elements and physical systems, Several schemes for improving reliability of physical systems.

Total Lecture Hours: (L=42, T=14)= 56</td></tr>
<tr><td>Text Books, and/or reference material</td><td colspan="7">Text Books:
1. S. H. Crandall, D. C. Karnopp, Dynamics of Mechanical and Electromechanical, Medtech Pub, 2017
2. J. Bentley, Principles of measurement systems. Pearson Education India; 3rd edition, 2002
Reference books:
1. A. Preumont Mechatronics, Dynamics of Electromechanical and Piezoelectric Systems, Springer, 2011
2. S. Banerjee, Dynamics for Engineers, Wiley; 1st edition, 2005
3. Research articles</td></tr>
</table>

MT/EC9053: Physical System Analysis and Modeling (Elective) [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	Understand characteristics of physical systems	1	3	1	3	1	1
CO 2	Apply quantitative analysis techniques to physical systems	3	3	3	3	1	2
CO 3	Understand modeling of physical systems	2	3	3	3	1	2
CO 4	Investigate complex designs of physical systems and case studies	3	3	3	3	1	2
Average		**2.25**	**3**	**2.5**	**3**	**1**	**1.75**

Department of Electronics and Communication Engineering							
Course Code	Title of the course	Program Core (PCR) / Electives (PEL)	**Total Number of contact hours: 56**				Credit
			Lecture (L)	Tutorial (T)	Practical (P)	Total Hours	
MT/EC9054	**Cyber Physical Electronic System Design**	PEL	3	1	0	4	4

Course Outcomes	After the completion of the course the student will be able to • **CO 1**: Understand application based electronic systems • **CO 2**: Understand basic building blocks of electronic systems • **CO 3**: Apply quantitative analysis techniques to electronic systems • **CO 4**: Learn fundamentals of cyber-physical electronic systems • **CO 5**: Investigate complex designs of cyber physical embedded systems through case studies
Topics Covered	**Module I. Introduction to cyber physical electronic system [L-1]** Concept of Cyber Physical Electronic Systems (CPES), Applications of CPES **Module II. Hardware Elements of Physical Systems [L-14; T-5]** Sensors, Resistive sensor, Capacitive sensors, Inductive sensors, Piezoelectric sensors, Piezoresistive sensors, MEMS sensors, MEMS Accelerometers, MEMS Gyro, Signal conditioning circuits, Signal Processing unit, Data presentation, Data storage, and Data communication units, Actuators, Motors, BLDC, Stepper Motors, Servo motors, AC motors, Linear actuators, Linear servo actuators, Mechanisms **Module III. Physical Embedded Systems [L-10; T-5]** Microcontrollers, Mini computers, Embedded systems, Vibration sensing, Force sensing, Pressure sensing, voltage sensing, Actuation systems, Open-loop system, Closed loop system, Embedded control strategies, Embedded PID controller. **Module IV. Physical Systems in Network [L-10; T-1]** Intranet, Internet, NFC, Bluetooth, Zigbee, WiFi, 4G, 5G, Industrial Ethernet, Industrial data communication Protocols, HART, MQTT, HTTP, Cyber physical systems, IoT, Industry 3.0, Industrial IoT **Module VI. Data Security Issues [L-1]** Requirement of data securities, Data encryption strategies. **Module VII. Case studies [L-6; T-3]** Cyber Physical motor speed control system, Cyber physical 3D printing systems, Cyber physical structural health monitoring systems, Industry 4.0. **Total Lecture Hours: (L=42, T=14)= 56**
Text Books, and/or reference material	**Text Books:** 1. J. Bentley, *Principles of measurement systems*. Pearson Education India; 3rd edition, 2002 2. E. A. Lee, S. A. Seshia, *Introduction to Embedded Systems - a Cyber Physical Systems Approach*, MIT Press; Second edition, 2019 3. B. A. Forouzan, *Data Communications and Networking*, McGraw Hill Education; 4th edition, 2017 **Reference books:** 1. A. Gilchrist *Industry 4.0 the industrial internet of things*, Apress; 1st edition, 2017 2. Research Articles

MT/EC9054: Cyber Physical Electronic System Design [Mapping between Course Outcomes (COs) and Program Outcomes (POs)]							
CO	**Statement**	**Program Outcomes**					
		PO 1	**PO2**	**PO3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	Understand application based electronic systems	2	3	1	3	1	1
CO 2	Understand basic building blocks of electronic systems	2	3	1	3	1	1
CO 3	Apply quantitative analysis techniques to electronic systems	2	3	1	3	1	1
CO 4	Understand fundamentals of cyber-physical electronic systems	3	2	2	1	1	3
CO 5	Investigate complex designs of cyber physical embedded systems through case studies	3	2	3	1	1	3
Average		**2.4**	**2.6**	**1.6**	**2.2**	**1**	**1.8**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9055</td><td>Electronic Measurements and System Design</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2" rowspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course the student will be able to
• CO 1: Understand concept of electronic measurements
• CO 2: Understand basic building blocks of electronic measurement systems
• CO 3: Apply quantitative analysis techniques to electronic measurement systems
• CO 4: Learn design techniques of electronic measurement systems
• CO 5: Investigate application specific measurement systems</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I: Introduction to measurements [L-1]

Module II: Static and dynamic characteristics [L-7; T-2]
Static characteristics of elements, Dynamic characteristics of elements, Quasi-static characteristics of elements, Static characteristics of systems, Dynamic characteristics of systems, linearity, non-linearity, Sensitivity, Resolution, Repeatability, Reproducibility, Response time, Settling time, Gain, bandwidth

Module III: Loading Effects in Measurements [L-4 ;T-2]
Loading effects in measurement systems, loading effect due to resistive sensors, Loading effect due to capacitive sensors, loading effect due to inductive sensors. Schemes to get rid of loading effects, two port representation of measurement systems.

Module IV: Error and Noise in Measurement systems [L-4; T-1]
Sources of noise in measurement systems, mathematical modelling of noise, environmental effects, Effects of Interfering and Modifying inputs, Error analysis, Systematic error, Random error. Statistical methods for noise and error analysis and Modelling.

Module V: Reliability analysis of measurement systems [L-4; T-1]
Concept of Reliability, Reliability of measurement systems, Reliability enhancement strategies

Module VI: Functional Elements of Measurement Systems [L-12; T-4]
Voltage sensors, Current sensors, Force sensors, Pressure sensors, Vibration sensors, Flow sensors, Motion Sensors, Magnetic flux sensors, Chemical sensors, Signal conditioning circuits, Bridge circuits, Amplifiers, Filters, Oscillators, ADC, Signal Processing Units, Microcontrollers, Data Presentation elements

Module VII: Case studies [L-10; T-4]
Flow measurement systems, Heat transfer effect and measurement systems, Optical measurement systems, Ultrasonic measurement systems, Gas chromatography.

Total Lecture Hours: (L=42, T=14)= 56</td></tr>
<tr><td>Text Books, and/or reference material</td><td colspan="7">Text Books:
4. J. Bentley, Principles of measurement systems. Pearson Education India; 3rd edition, 2002
5. Ernest O. Doebelin, Dhanesh N. Manik, Doebelin's "Measurement Systems" 7th Edition McGraw-Hill; Seventh edition, 2019</td></tr>
</table>

6. David A. Bell, "*Electronic Instrumentation and Measurements"*, Oxford University Press India; Third edition, 2013

Reference books:

1. Research Articles

MT/EC9055: Electronic Measurements and System Design (Elective) **[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]**							
CO	**Statement**	**Program Outcomes**					
		PO1	**PO2**	**PO3**	**PSO 1**	**PSO 2**	**PSO 3**
CO 1	Understand concept of electronic measurements	2	3	1	3	1	1
CO 2	Understand basic building blocks of electronic measurement systems	2	3	1	3	1	2
CO 3	Apply quantitative analysis techniques to electronic measurement systems	2	3	1	3	1	1
CO 4	Learn design techniques of electronic measurement systems	3	2	2	3	1	3
CO 5	Investigate application specific measurement systems	3	2	3	3	1	3
Average		**2.4**	**2.6**	**1.6**	**3**	**1**	**2**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9056</td><td>DSP Architectures in VLSI</td><td>CORE</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td>Course Objectives</td><td colspan="7">This course is designed to give a comprehensive coverage of the VLSI architectures for digital signal processing. The central theme of the course is to design efficient VLSI architectures for computing algorithms frequently encountered in DSP systems. It focuses on algorithm transformation and architecture design techniques to improve the design with high throughput, less area, and power.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course, the student will be able to:
• CO 1: State VLSI design methodology for signal processing systems.
• CO 2: Describe VLSI algorithms and architectures for DSP.
• CO 3: Implement/Simulate basic architectures for DSP using Matlab/CAD tools.
• CO 4: Discuss various issues that need to be addressed when implementing DSP algorithms in real hardware with finite resources such as processing speed, memory, and bit resolution.
• CO 5: Analyze DSP architectures and evaluate their performance.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction to Digital Signal Processing [L – 7; T - 2]
Review of DSP fundamentals: Discrete Systems: Representation of Systems, Properties of DSP systems, Difference equation and its relationship with system function, Impulse response and frequency response.

Module II. Digital Signal Processing Algorithms [L – 8; T - 2]
Introduction for DSP algorithms: VLSI Design flow, Mapping algorithms into Architectures: Graphical representation of DSP algorithms – signal flow graph (SFG), data flow graph (DFG), critical path, dependence graph (DG). Data path synthesis, control structures, Optimization at Logic Level and architectural level, Retiming.

Module III. Introduction to DSP systems [L – 6; T - 2]
DSP Systems, Parallel and pipeline of signal processing application: Architecture for real-time systems, latency and throughput related issues, clocking strategy, array architectures; Pipelining processing of Digital filter, Parallel processing, Parallel and pipelining for Low power design, ASIC design.

Module IV. Systolic Array Architecture [L – 5; T - 2]
Methodology of systolic array architecture, FIR based Systolic Array, Selection of Scheduling Vector, Matrix multiplication of systolic array.

Module V. Signal Processing Architectures [L – 7; T - 2]
Convolution technique, Retiming concept, Folding/Unfolding Transformation, Fast convolution, Cook-Toom algorithm, modified Cook-Toom algorithm. Winograd Algorithm.

Module VI. Scaling and Round-off Noise [L – 5; T - 2]
Scaling and round-off noise, scaling operation, round-off noise, state variable description of digital</td></tr>
</table>

	filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters. **Module VII. Low Power Design [L – 4; T - 2]** Theoretical background, Scaling v/s power consumption, power analysis, Power estimation approach, Power reduction techniques. **Total Contact Hours: (L=42, T=14)= 56**
Text Books, and/or Reference Materials	**Text Books:** 1. Keshab K. Parhi, "*VLSI Digital Signal Processing Systems, Design and Implementation*", Wiley-Interscience, 1999. **Reference Books:** 1. Uwe Meyer-Baese, "*Digital Signal Processing with Field Programmable Gate Arrays*", Springer, Third Edition, 2007.

MT/EC9056: DSP Architectures in VLSI
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	State VLSI design methodology for signal processing systems.	2	1	2	3	1	1
CO2	Describe VLSI algorithms and architectures for DSP.	2	3	1	3	2	2
CO3	Implement/Simulate basic architectures for DSP using Matlab/CAD tools.	3	2	1	2	2	1
CO4	Analyze DSP architectures and evaluate their performance.	3	1	1	3	2	1
CO5	Discuss various issues that need to be addressed when implementing DSP algorithms in real hardware.	3	1	1	2	1	2
Average		**2.50**	**1.50**	**1.50**	**2.67**	**1.50**	**1.33**

<table>
<tr><td colspan="7">Department of Electronics & Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the Course</td><td rowspan="2">Program Core (PCR) / Elective (PEL)</td><td colspan="4">Total contact hours : 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9057</td><td>Power Management IC Design</td><td>Elective (PEL)</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">)</td><td colspan="5"></td></tr>
<tr><td colspan="3"></td><td colspan="5"></td></tr>
<tr><td>Course Objective</td><td colspan="7">The course is to develop understanding of why power management circuits are needed in a VLSI system. It primarily deals with different components of a power management system with focus on dc-dc converters. It aims to design a chip level dc-dc converter from the given specifications.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After successful completion of the course, the student will be able to::
• CO 1: Define different types of DC-DC converters.
• CO 2: Describe the concept of power management ICs.
• CO 3: Employ Miller compensation to obtain better time response.
• CO 4: Design a compensator for Buck converter.
• CO 5: Compare between Buck and Boost Converter.
• CO 6: Evaluate the performance of a Switched Capacitor DC-DC Converter.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I. Introduction [L – 6; T - 2]
Introduction to Power Management -Voltage regulators, Need of DC-DC Converters, Types of DC-DC Converters, Linear versus Switching Regulator, Performance Parameters - Efficiency, Accuracy, Line and Load Regulation, Line and Load Transient response, PSRR; Point-of-Load Regulator.

Module II. Linear Regulators [L – 8; T - 3]
Bandgap Voltage Reference, Low Drop-Out Regulator (LDO), Source and sink regulators, shunt regulator, pass transistor, error amplifier, small signal and stability analysis, compensation techniques, current limiting, power supply rejection ratio (PSRR), NMOS vs. PMOS regulator, current regulator.

Module III. Switching Regulator [L – 8; T - 3]
Basic Concept of a Switching Regulator, Synchronous and Non-Synchronous Switching Converters; PWM Control Techniques, Control Techniques for DC-DC Converters; Small-Signal Modeling of a DC-DC Converter, Loop Gain and Stability Analysis using Continuous-Time Model.

Module IV. Top-down Design of DC-DC Converter [L – 7; T - 2]
Topology selection, Switching frequency and external component selection; designing gate driver, PWM modulator, error amplifier, oscillator, ramp generator, feedback resistors, current sensing, current limit and short circuit protection, chip level layout guidelines.

Module V. Buck Boost Converter [L – 7; T - 3]
Introduction to the Buck-Boost Converter, Introduction to Switched-Capacitor DC-DC Converters, Applications of SC DC-DC Converters in Open-Loop, Output Regulation in SC DC-DC Converters using Feedback Control.

.</td></tr>
</table>

	Module VI. Advanced Topics [L – 6; T - 1] Digitally controlled dc-dc converters, digitally controlled LDOs, adaptive compensation, dynamic voltage scaling (DVS), Single-Inductor Multiple-Outputs (SIMO) Converters. **Total Lecture Hours: (L=42, T=14)=56**
Text Books, and/or Reference Materials	**Text Books:** 1. Christophe P. Basso, "*Switch-Mode Power Supplies: SPICE Simulations and Practical Designs*", McGraw-Hill Professional, 2008. 2. Behzad Razavi, "*Design of Analog CMOS Integrated Circuits*", McGraw-Hill, 2017 **Reference Books:** 1. Ke-Horng Chen, "*Power Management Techniques for Integrated Circuit Design*", Wiley-Blackwell, 2016. 2. Robert W. Erickson, Dragan Maksimovic, "*Fundamentals of Power Electronics*", 2nd edition Springer, 2001.

MT/EC9057: Power Management IC Design
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	Define different types of DC-DC converters	2	2	2	2	3	2
CO2	Explain techniques of Stabilizing a Regulator..	2	1	2	2	3	1
CO3	Employ Miller compensation to realize good phase margin	1	2	1	2	3	3
CO4	Design a compensator for Buck converter.	2	1	2	3	3	1
CO5	Compare between Buck and Boost Converter	1	1	2	3	3	2
CO6	Evaluate the performance of a Switched Capacitor DC-DC Converter	1	2	3	3	3	1
Average		**1.5**	**1.5**	**2**	**2.5**	**3**	**1.67**

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 56</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>MT/EC9058</td><td>Smart Materials based Electronic Devices</td><td>PEL</td><td>3</td><td>1</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2"></td><td colspan="6"></td></tr>
<tr><td colspan="2"></td><td colspan="6"></td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After the completion of the course the student will be able to
• CO 1: Understand concept of Smart Materials based Electronic Devices
• CO 2: Apply quantitative analysis techniques to Smart Materials based Electronic Devices
• CO 3: Understand basic building blocks of Smart Materials based Electronic systems
• CO 4: Learn design techniques of Smart Materials based Electronic systems
• CO 5: Investigate application specific Smart Materials based Electronic systems</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Module I: Introduction to Smart Materials based Electronic Devices [L-1]
Smart Materials, Smart Materials based Electronic Devices, Applications of Smart Materials based Electronic Devices

Module II: Characteristics of Smart Materials based Electronic Devices [L-7; T-1]
Static, dynamic and quasi static characteristics of Smart Materials based Electronic Devices

Module III: Analysis and Modelling of Smart Materials based Electronic Devices [L-12; T-5]
Energy, Co-energy, Energy methods, Hamilton’s principle, Lagrange's Equations, Analysis and modelling of Smart material based electromechanical devices

Module IV: Piezoelectric Devices [L-8; T-4]
Piezoelectric sensors, actuators, transformers, motors, resonators

Module V: Shape Memory Alloy devices [L-4; T-1]
Shape Memory effect , Shape Memory Alloy elements, Shape Memory Alloy elements as actuators, Shape Memory Alloy element as sensor

Module VI: Electroactive polymer devices [L-3; T-1]
Electroactive polymers, Electroactive polymer actuators

Module VII: FEM Modelling of Smart Materials based Electronic Devices [L-2]
Concept of FEM, FEM-based CAD software for Smart materials based electronic Devices

Module VIII: Case studies [L-5;T-2]
Piezoelectric transducers for ultrasound generation, SMA actuator driven finger exoskeleton

Total Lecture Hours: (L=42, T=14)= 56</td></tr>
<tr><td>Text Books, and/or reference material</td><td colspan="7">Text Books:
1. V. K.Varadan, K. J. Vinoy, S. Gopalakrishnan, “Smart Material Systems and MEMS: Design and Development Methodologies”, Wiley, 2006
2. J. Bentley, Principles of measurement systems. Pearson Education India; 3rd edition, 2002
3. S. H. Crandall, D. C. Karnopp, Dynamics of Mechanical and Electromechanical, Medtech Pub, 2017

Reference books:
1. D. J. Leo, Engineering Analysis of Smart Material Systems, John Wiley & Sons Inc, 2007</td></tr>
</table>

2. A. Preumont *Mechatronics, Dynamics of Electromechanical and Piezoelectric Systems*, Springer, 2011
3. D. K. Gehmlich, S. B. Hammond, *Electromechanical system*, McGraw-Hill, 1967
4. D. Hutton, *Fundamentals of Finite Element Analysis*, McGraw Hill, 2003
5. Research articles

MT/EC9058: Smart Materials based Electronic Devices
[Mapping between Course Outcomes (COs) and Program Outcomes (POs)]

CO	Statement	Program Outcomes					
		PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Understand concept of Smart Materials based Electronic Devices	3	3	3	1	1	1
CO 2	Apply quantitative analysis techniques to Smart Materials based Electronic Devices	2	3	2	3	1	2
CO 3	Understand basic building blocks of Smart Materials based Electronic systems	3	3	3	3	1	1
CO 4	Learn design techniques of Smart Materials based Electronic systems	3	3	2	3	2	3
CO 5	Investigate application specific Smart Materials based Electronic systems	2	3	2	2	1	2
Average		2.6	3	2.4	2.4	1.2	1.8